UNIT-I

LOW – FREQUENCY SINGLE – STAGE AMPLIFIERS

Objectives

- To introduce basic structures of MOSFET and BJT amplifier circuits.
- To familiarize with characteristic parameters of amplifiers
- To design and analyse behaviour of BJT & FET amplifiers at low frequencies.

Syllabus

MOS Amplifiers, The basic structure, characterizing MOS amplifiers, low - frequency response of common source (CS) amplifier,common source (CS) amplifier with a source resistance, design of CS amplifier, BJT amplifiers, The basic structure, characterizing BJT amplifiers, low – frequency response of the common emitter (CE) amplifier,common emitter (CE) amplifier with an emitter resistance, design of CE amplifier.

Pre-requisites

- Small-signal models of MOSFET
- Small-signal models of BJT
- Circuit models for amplifiers
- The terms: Frequency response and Bandwidth of an amplifier

Outcomes:

Students will be able to

- distinguish unilateral and non-unilateral amplifiers
- analyse FET and BJT amplifiers at low frequencies
- design CE and CS amplifiers at low frequencies

Pre-requisites

- **Small – signal equivalent circuit models of MOSFET**

- From a signal point of view the FET behaves as a Voltage Controlled current source. It accepts a signal V_{GS}between gate and source and provides a current g_mV_{GS}, at the drain terminal.
- The input resistance of this controlled source is very high – ideally infinite. The output resistance – i.e., resistance looking in to the drain – also is high.
- Putting all of this together, we get the circuit in as shown in below figurethat represents the small signal model or small signal equivalent circuit.

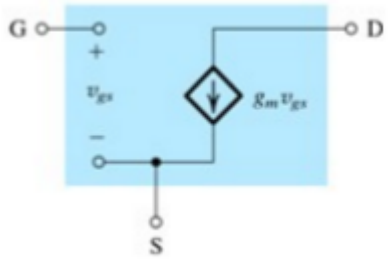


Fig. Small signal model for the MOSFET neglecting the dependence of i_D on V_{DS} in saturation

- In the analysis of a MOSFET amplifier circuit, transistor can be replaced by the equivalent model. Ideal constant DC voltage sources are replaced by short circuit, and Ideal constant DC current sources are replaced by an open circuit in the small signal model.
- Another approach of the small signal model of amplifier is that assume the drain current in saturation is independent of the drain voltage. From MOSFET characteristics in saturation, we know that the drain current does in fact depend on V_{DS} in linear manner. Such linear relation was modeled by a finite resistance r_o between drain and source. we represent it as

$$r_o = \frac{|V_A|}{I_D}$$

- The current I_D is the value of the DC drain current without the channel –length modulation taken into account ; that is,

$$I_D = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2$$

- Accuracy of the small signal model can be improved by including r_o in parallel with the controlled source.

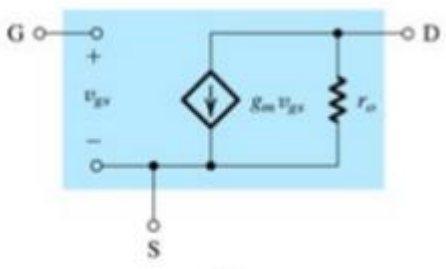


Fig.Small signal model for MOSFET including the effect of channel –length modulation.

- It is important to note that small signal model parameters $g_m$and $r_o$depend on the DC bias point of the MOSFET.
- MOSFET amplifier voltage gain expression

$$A_v = \frac{v_d}{v_{gs}} = -g_m(R_D // r_o)$$

- Thus finite output resistance r_o results in a reduction in the magnitude of voltage gain.
- All the above analysis performed on an NMOS transistor, apply equally well to PMOS device, except for using V_{GS}, V_t ,V_{OV} , andV_A and replacing k_n' with k_p'.

The T Equivalent Circuit Model

- It is possible to develop an alternate equivalent circuit model for the MOSFET. The development of such model is known as T model.Figure (a) shows the equivalent circuit of MOSFET without r_o.
- In the figure as shown below, we have added a second $g_m V_{gs}$current source in series with the original controlled source. This addition of current source does not change the terminal currents.
- The newly created circuit node, labeled as X , is joined to the gate terminal G. Observe that the gate current doesn't change(remains equal to zero)-thus this connection doesn't alter the terminal characteristics.
- We have a controlled voltage source $g_m v_{gs}$connected across its control voltage vgs. We can replace this controlled source by a resistance as long as this resistance draws an equal current as the source. Thus the value of resistance is $v_{gs}/g_m v_{gs} = 1/g_m$. This replacement is shown in figure (d)
- Observe that*ig* is still zero, $i_d = g_m v_{gs}$and is=$v_{gs}/(1/g_m)$ =$g_m v_{gs}$, all same as the original model in figure (c)
- Note that the resistance between gate and source, looking into the gate, is infinite. This observation useful in many applications.

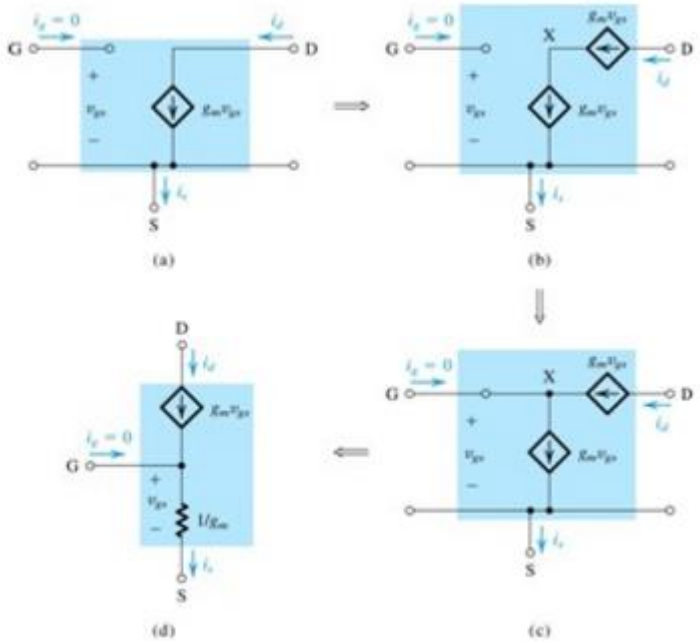


Fig.Development of the T equivalent – circuit model for the MOSFET. For simplicity, r_o has been omitted but can be added between D and S in the T model of (d).

- In T-model including resistance r_o between drain and source the circuit is modeled as follows.

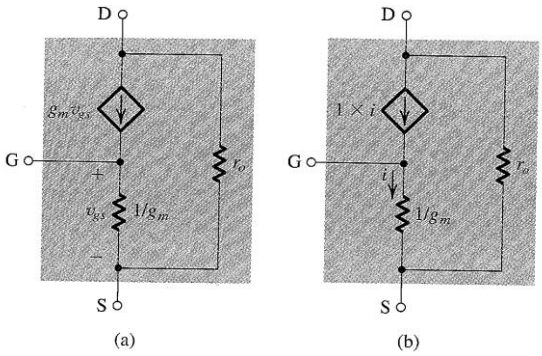


Fig.(a)The T model of the MOSFET augmented with the drain to source resistance r_o; (b) An alternative representation of the T model.

- **Small signal equivalent circuit models of BJT**

The Hybrid – π Model

An equivalent circuit model for the BJT is shown in below fig

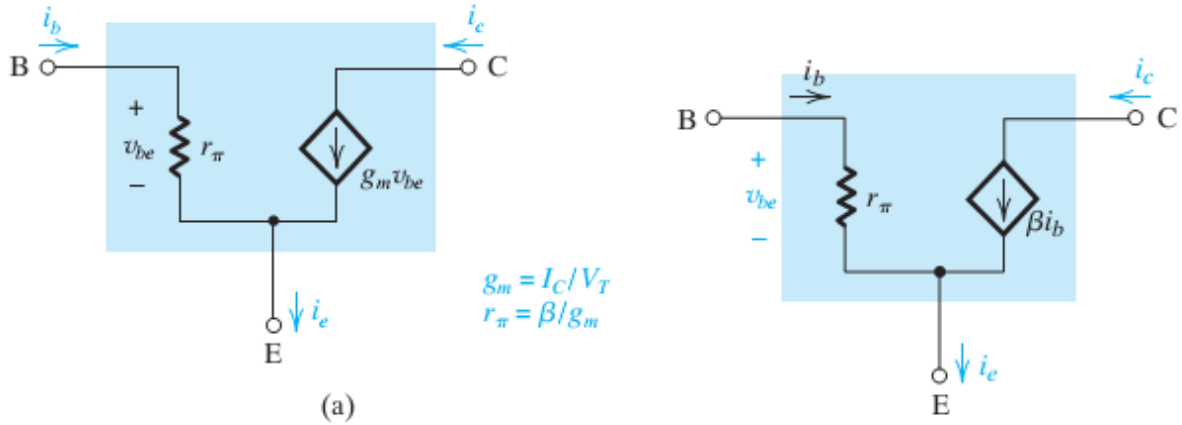


Fig. Two slightly different versions of the simplified hybrid –π model for the small signal operation of the BJT. The equivalent circuit in (a) represents the BJT as a voltage controlled current source (a transconductance amplifier), and that in (b) represents the BJT as a current controlled current source (a current amplifier).

- Model (a) represents the BJT as a voltage controlled current source and explicitly includes the input resistance looking into the base r_π. The model obviously yields $i_c = g_m v_{be}$ and $i_b = v_{be}/r_\pi$.
- At the emitter node we have

$$i_e = \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi}(1 + g_m r_\pi)$$
$$= \frac{v_{be}}{r_\pi}(1 + \beta) = v_{be} \Big/ \left(\frac{r_\pi}{1+\beta}\right)$$
$$= v_{be}/r_e$$

- A slightly different circuit model(b) can be obtained by expressing the current of the controlled source ($g_m v_{be}$) in terms of the base current i_b(current controlled current source) as follows:

$$g_m v_{be} = g_m(i_b r_\pi)$$
$$= (g_m r_\pi) i_b = \beta i_b$$

- The two models (a & b) are the simplified hybrid –π model for the small signal operation for the BJT. The model parameters g_m, r_π depend on the value of the DC bias current Ic.
- Finally, although the models have been developed for an NPN transistor, they apply equally well to a PNP transistor with no change of polarities.

The T Model

- Although hybrid –π model can be used to carry out small signal analysis of all transistor circuits, there are situations in which alternative model shown in below fig, is much more convenient, is called as T model.

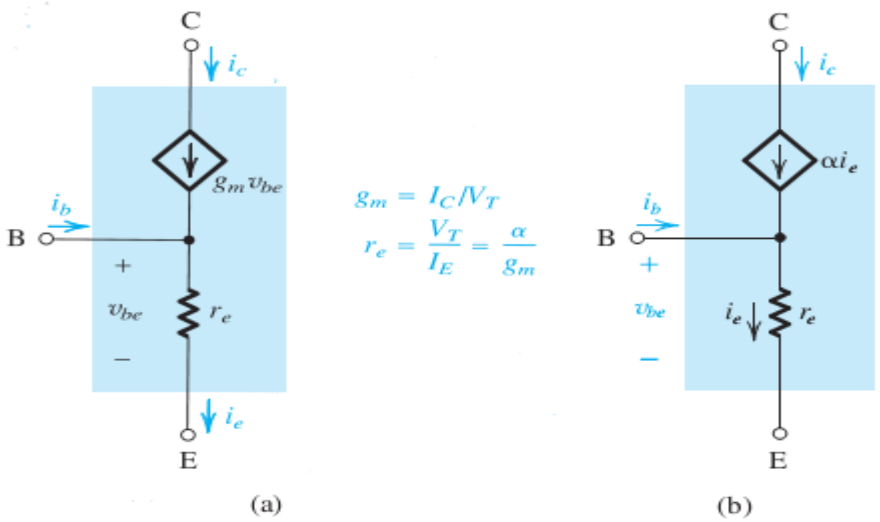


Fig. Two slightly different versions of what is known as the T model of the BJT. The circuit in (a) is a voltage controlled current source representation and that in (b) is a current controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid –π model.

- The two versions of T-model shown in above figure. Fig. (a) represents the BJT as a voltage controlled current source with the control voltage being v_{be}. Here, however, the resistance between base and emitter, looking into the emitter, is explicitly shown.
- From fig(a) we see clearly that the model yields the correct expression for i_c and i_b. For i_b we note that at the base node we have

$$i_b = \frac{v_{be}}{r_e} - g_m v_{be} = \frac{v_{be}}{r_e}(1 - g_m r_e)$$

$$= \frac{v_{be}}{r_e}(1 - \alpha) = \frac{v_{be}}{r_e}\left(1 - \frac{\beta}{\beta+1}\right)$$

$$= \frac{v_{be}}{(\beta+1)r_e} = \frac{v_{be}}{r_\pi}$$

- If in the model of Fig (a) the current of the controlled source is expressed in terms of the emitter current as follows :

$$g_m v_{be} = g_m(i_e r_e)$$

$$= (g_m r_e) i_e = \alpha i_e$$

- We obtain alternative T-model shown in Fig (b). Here the BJT is represented as a current – controlled current source but with the control signal being i_e.

- **Circuit models for Amplifiers**

Irrespective of complexity of the amplifier circuit, circuit can be represented as a building block in a system one must able to characterize, or model its terminal behaviour. In this section we will study simple but effective amplifier models.

Voltage Amplifiers

- The model consists of Voltage controlled voltage source having a gain of factor of A_{vo}
- An input resistance R_i that accounts for amplifier draws an input current from the signal source.
- Output Resistance R_o that accounts for the change in output voltage as the amplifier is called upon to supply output current to load.

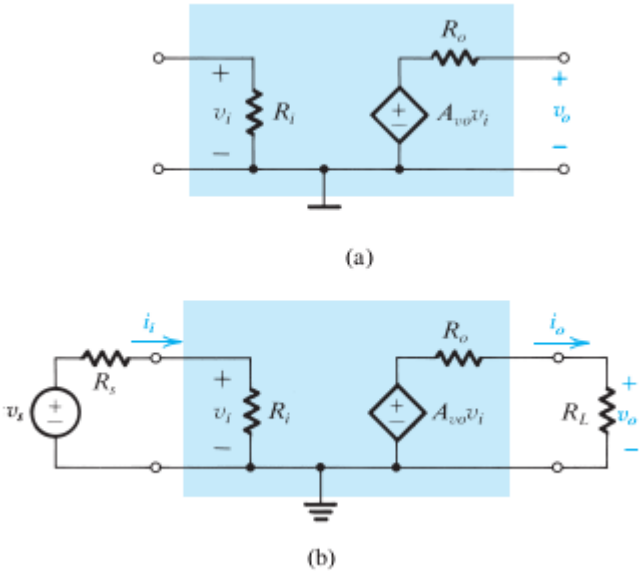


Fig.a) Circuit model for voltage amplifier, b) Voltage amplifier with input signal source and load

- A signal voltage source V_s having a resistance R_s connected to at the output to a load resistance R_L.
- The non-zero output resistance R_o causes only a fraction of $A_{vo}V_i$ to appear across the output.
- Using voltage division rule we obtain

$$v_o = A_{vo} v_i \frac{R_L}{R_L + R_o}$$

Thus the voltage gain is given by

$$A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o}$$

- In order not to lose gain in coupling the amplifier output to load, the output resistance R_o should be much smaller than the load resistance R_L or to keep the output voltage v_o as constant as possible.

- An ideal voltage amplifier is one with $R_o=0, R_L=\infty$, then $A_v=A_{vo}$. Where, A_{vo} is the voltage gain of the unloaded amplifier, or open circuit voltage gain.
- The finite input resistance R_i introduces another voltage divider action at the input, with the result that only a fraction of the source signal V_s actually reaches the input terminals of the amplifier; that is

$$v_i = v_s \frac{R_i}{R_i + R_s}$$

- The overall voltage gain (V_o/V_s) can be found

$$\frac{v_o}{v_s} = A_{vo} \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o}$$

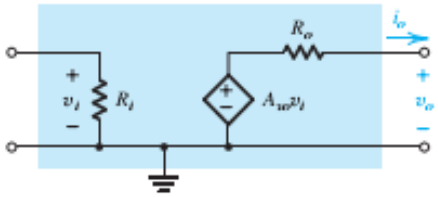
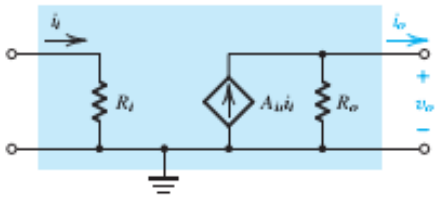
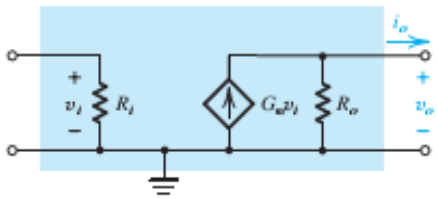
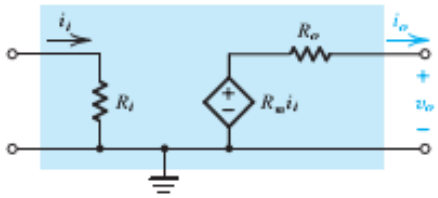
Cascaded Amplifiers

- To meet given amplifier specifications the need often arises to design the amplifier as a cascade of two or more stages. The stages are not usually identical. To illustrate the analysis and design of cascade amplifiers, we consider a practical example.

Other Amplifier Types

- The below table shows the four amplifier types, their circuit models ,the definition of their gain parameters, and the ideal values of their input and output resistances.

Table The Four Amplifier Types

Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		Open-Circuit Voltage Gain $A_{vo} \equiv \left.\frac{v_o}{v_i}\right\|_{i_o=0}$ (V/V)	$R_i = \infty$ $R_o = 0$
Current Amplifier		Short-Circuit Current Gain $A_{is} \equiv \left.\frac{i_o}{i_i}\right\|_{v_o=0}$ (A/A)	$R_i = 0$ $R_o = \infty$
Transconductance Amplifier		Short-Circuit Transconductance $G_m \equiv \left.\frac{i_o}{v_i}\right\|_{v_o=0}$ (A/V)	$R_i = \infty$ $R_o = \infty$
Transresistance Amplifier		Open-Circuit Transresistance $R_m \equiv \left.\frac{v_o}{i_i}\right\|_{i_o=0}$ (V/A)	$R_i = 0$ $R_o = 0$

Frequency Response of Amplifiers

- An important characterization of an amplifier in terms of its response to input sinusoids of different frequencies. Such characterization of amplifier performance is known as the amplifier frequency response.

Amplifier bandwidth

- The band of frequncies over which the gain of the amplifier is almost constant,to within a certain number of decibels(usually 3dB),is called the Amplifier bandwidth.

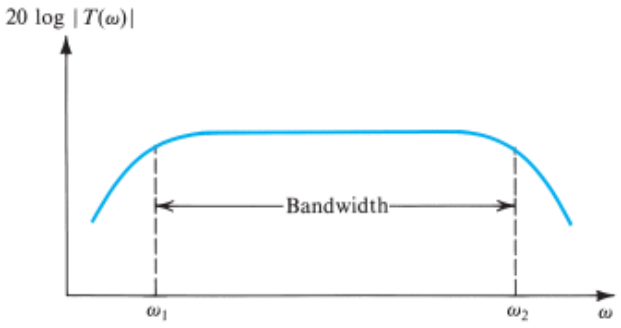


Fig. Typical magnitude response of amplifier.

SYLLABUS

1.1 Low – frequency Single-stage MOS amplifiers

MOS amplifiers

- In discrete circuits the MOSFET source is usually tied to the substrate, the body effect will be absent. Therefore we shall *not* take the body effect into account. Also, in some circuits we will neglect r_0 in order to keep the analysis simple.

1.1.1 The Basic Structure

- Figure 1.1 shows the basic circuit to implement the various configurations of discrete-circuit MOS amplifiers. Among the various schemes for biasing discrete MOS amplifiers, the constant-current biasing is employed for its effectiveness and simplicity. Figure 1.1 indicates the dc current and the dc voltages resulting at various nodes.

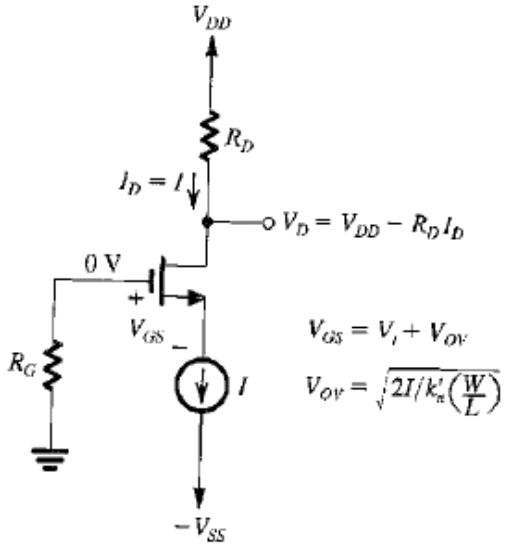


Fig.1.1: Basic structure of the circuit used to realize single-stage discrete-circuit MOS amplifier configurations.

1.1.2 Characterizing Amplifiers

- Most of the amplifiers are non-unilateral amplifiers, i.e., they have internal feedback that may cause their input resistance to depend on the load resistance. Similarly, internal feedback may cause the output resistance to depend on the value of the resistance of the signal source feeding the amplifier. A number of remarks are in order:
- The amplifier is shown fed with a signal source having an open-circuit voltage v_{sig} and an internal resistance R_{sig}. These can be the parameters of an actual signal source or the Thevenin equivalent of the output circuit of another amplifier stage preceding the one under study in a cascade amplifier. Similarly, R_L can be an actual load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.

- Parameters R_t, R_0, A_{v0}, A_{is}, and G_m pertain to the amplifier proper; that is, they do not depend on the values of R_{sig} and R_L. By contrast, R_{in}, R_{out}, A_v, A_t, G_{v0}, and G_v may depend on one or both of R_{sig} and R_L. Also, observe the relationships of related pairs of these parameters; for instance,

$$R_i = R_{in}|_{R_L=\infty}, \text{ and } R_o = R_{out}|_{R_{sig}=0}.$$

- For non-unilateral amplifiers, R_{in} may depend on R_L, and Rout may depend on R_{sig}. No such dependencies exist for unilateral amplifiers, for which $R_{in} = R_i$ and Rout = R_0.
- The loading of the amplifier on the signal source is determined by the input resistance R_{in}. The value of R_{in} determines the current that the amplifier draws from the signal source. It also determines the proportion of the signal v_{sig} that appears at the input of the amplifier proper (i.e., v_t).
- When evaluating the gain Av from the open-circuit value A_{v0}, R_0 is the output resistance. This is because Av is based on feeding the amplifier with an ideal voltage signal vt.
- If the overall voltage gain G_v is to be calculated from its open-circuit value G_{v0}, the output resistance to use is Rout. This is because G_v is based on feeding the amplifier with vsig, which has an internal resistance Rsig.

1.1.3 Low – frequency response of the Common-Source (CS) Amplifier

- The common-source (CS) or grounded-source configuration is the most widely used of all MOSFET amplifier circuits. A common-source amplifier realized using the circuit of Fig. 1.1 is shown in Fig. 1.2 (a).
- Observe that to establish a **signal ground,** or an **ac ground** as it is sometimes called, at the source, we have connected a large capacitor, C_S, between the source and ground. This capacitor, usually in the *pF* range, is required to provide a very small impedance (ideally, zero impedance; i.e., in effect, a short circuit) at all signal frequencies of interest.
- In this way, the signal current passes through $C_S$to ground and thus *bypasses* the output resistance of current source *I*(and any other circuit component that might be connected to the MOSFET source); hence, *Cs* is called a **bypass capacitor.**
- The lower the signal frequency, the less effective the bypass capacitor becomes. Here we shall assume that $C_S$is acting as a perfect short circuit and thus is establishing a zero signal voltage at the MOSFET source.
- In order not to disturb the dc bias current and voltages, the signal to be amplified, shown as voltage source *v$ig*with an internal resistance R_{sig}, is connected to the gate through a large

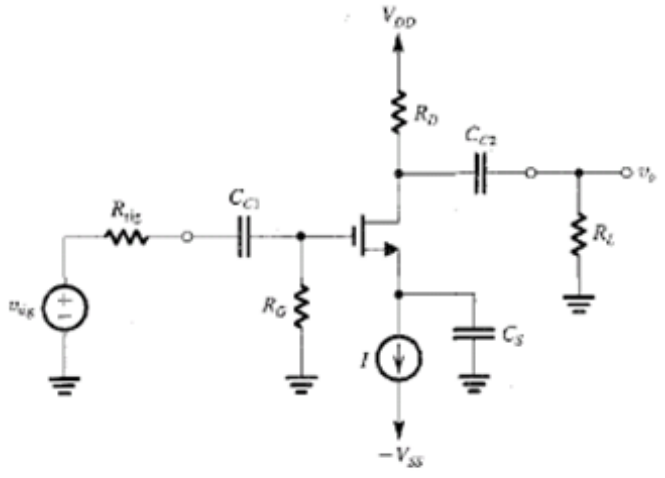
capacitor C_{C1} . Capacitor C_{C1}, known as a **coupling capacitor,** is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc.

- As the signal frequency is lowered, the impedance of C_{C1} (i.e., $1/j\omega C_{C1}$) will increase and its effectiveness as a coupling capacitor will be correspondingly reduced.
- Here we assume $C_{C1}$is acting as a perfect short circuit as far as the signal is concerned. Before leaving C_{C1}, where the signal source can provide an appropriate dc path to ground, the gate can be connected directly to the signal source and both $R_G$and C_{C1}can be dispensed with.
- The voltage signal resulting at the drain is coupled to the load resistance $R_L$via another coupling capacitor C_{C2}. We assume that C_{C2}acts as a perfect short circuit at all signal frequencies of interest and thus that the output voltage $v_0 = v_d$.
- Note that $R_L$can be either an actual load resistor, to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of another amplifier stage in cases where more than one stage of amplification is needed.
- To determine the terminal characteristics of the CS amplifier—that is, its input resistance, voltage gain, and output resistance—we replace the MOSFET with its small-signal model. The resulting circuit is shown in Fig. 1.2 (b).
- This amplifier is unilateral. Therefore Rin does not depend on R_L, and thus $R_{in}= R_i$. Also, Rout will not depend on R_{sig}, and thus $R_{out} = R_0$. Analysis of this circuit is straight forward and proceeds in a step-by-step manner, from the signal source to the amplifier load. At the input

$$i_g = 0$$

$$R_{in} = R_G$$

$$v_i = v_{sig}\frac{R_{in}}{R_{in} + R_{sig}} = v_{sig}\frac{R_G}{R_G + R_{sig}}$$



(a)

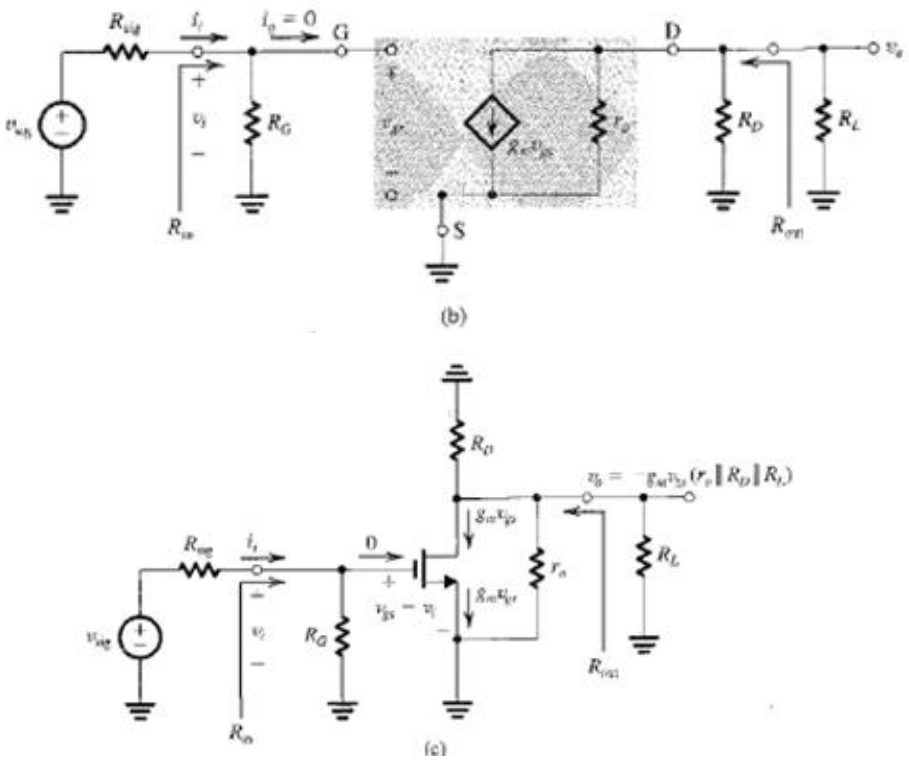


Fig. 1.2: (a) Common-source amplifier based on the circuit of Fig. 1.1, (b) Equivalent circuit of the amplifier for small-signal analysis, (c) Small-signal analysis performed directly on the amplifier circuit with the MOSFET model implicitly utilized.

- Usually $R_G$is selected very large (e.g., in the MΩ range) with the result that in many applications $R_C >> R_{sig}$and

$$v_i \cong v_{\text{sig}}$$

$$v_{gs} = v_i$$

$$v_o = -g_m v_{gs}(r_o \| R_D \| R_L)$$

Thus the voltage gain $A_v$is

$$A_v = -g_m(r_o \| R_D \| R_L)$$

and the open-circuit voltage gain $A_{vo}$is

$$A_{vo} = -g_m(r_o \| R_D)$$

The overall voltage gain from the signal-source to the load will be

$$G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} A_v$$

$$= -\frac{R_G}{R_G + R_{\text{sig}}} g_m(r_o \| R_D \| R_L)$$

- Finally, to determine the amplifier output resistance R_{out} we set v_{sig} to 0; that is, we replace the signal generator v_{sig} with a short circuit and look back into the output terminal, as indicated in Fig. 1.2.

$$R_{out} = r_o \| R_D$$

- Including the output resistance v_0 in the analysis of the CS amplifier is straight forward: Since r_0 appears between drain and source, it in effect appears in parallel with R_D. Since it is usually the case that $r_0 >> R_D$, the effect of r_0 will be a slight decrease in the voltage gain and a decrease in Rout.

- Although small-signal equivalent circuit models provide a systematic process for the analysis of any amplifier circuit. Consider the Fig. 1.2 (c) the small-signal analysis of the CS amplifier performed on a somewhat simplified version of the circuit and its equivalent circuit is shown in Fig. 1.2 (b). The CS amplifier has a very high input resistance, a moderately high voltage gain, and a relatively high output resistance.

1.1.4 The Common-Source Amplifier with a Source Resistance

- Here a resistance R_S in the source lead of the common-source amplifier, as shown in Fig. 1.3 (a). The corresponding small-signal equivalent circuit is shown in Fig. 1.3 (b) where we note that the transistor has been replaced by its T equivalent-circuit model.
- The T model is used in preference to the π - model because it makes the analysis simpler. In general, whenever a resistance is connected in the source lead, as for instance in the source-follower circuit, the T model is preferred: The source resistance then simply appears in series with the resistance $1/g_m$ which represents the resistance between source and gate, looking into the source.
- We have not included r_0 in the equivalent-circuit model. Including r_0 would complicate the analysis considerably; r_0 would connect the output node of the amplifier to the input side and thus would make the amplifier non-unilateral.
- From Fig. 1.3 (b) we see that as in the case of the CS amplifier,

$$R_{in} = R_i = R_G$$

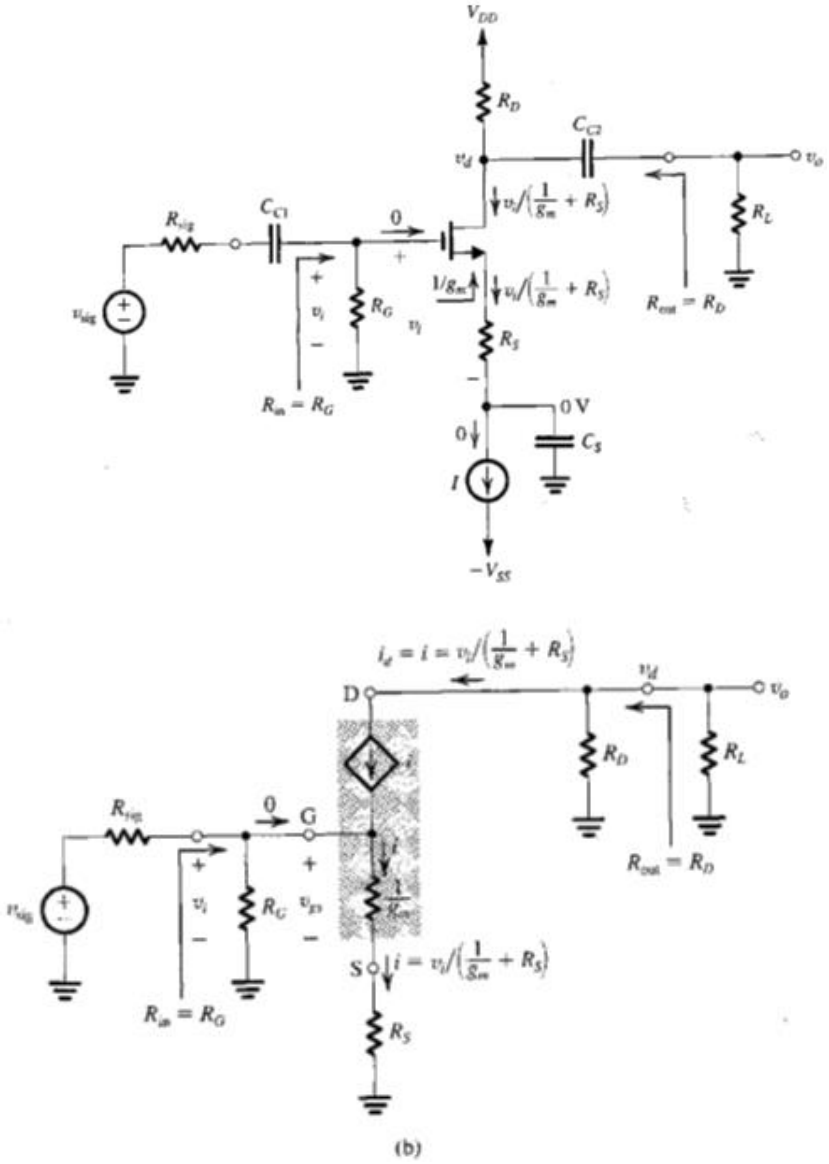
$$v_i = v_{sig}\frac{R_G}{R_G + R_{sig}}$$

- Unlike the CS circuit, however, here v_{gs} is only a fraction of v_I. It can be determined from the voltage divider composed of $1/g_m$ and R_S that appears across the amplifier input as follows:

$$v_{gs} = v_i \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_S} = \frac{v_i}{1 + g_m R_S}$$

- Thus we can use the value of R_S to control the magnitude of the signal v_{gs} and thus ensure that v_{gs} does not become too large and cause unacceptably high nonlinear distortion. This is the first benefit of including resistor R_S.
- R_S causes the useful bandwidth of the amplifier to be extended. The mechanism by which Rs causes such improvement in amplifier performance is that of negative feedback. The current i_d is equal to the current i flowing in the source lead; thus,

$$i_d = i = \frac{v_i}{\frac{1}{g_m} + R_S} = \frac{g_m v_i}{1 + g_m R_S}$$



(b)

Fig. 1.3: (a) Common-source amplifier with a resistance R_S in the source lead, (b) Small-signal equivalent circuit with r_0 neglected.

- Thus including R_S reduces i_d by the factor $(1 + g_m R_S)$, since this is the factor relating v_{gs} to v_i and the MOSFET produces $i_d = g_m v_{gs}$. The above drain current equation indicates also that the effect of RS can be thought of as reducing the effective g_m by the factor $(1 + g_m R_S)$.
- The output voltage can now be found from

$$v_o = -i_d(R_D \| R_L)$$
$$= -\frac{g_m(R_D \| R_L)}{1 + g_m R_S} v_i$$

- Thus the voltage gain is

$$A_v = -\frac{g_m(R_D \| R_L)}{1 + g_m R_S}$$

And setting $R_L = \infty$ gives

$$A_{vo} = -\frac{g_m R_D}{1 + g_m R_S}$$

- The overall voltage gain G_0 is

$$G_v = -\frac{R_G}{R_G + R_{sig}} \frac{g_m(R_D \| R_L)}{1 + g_m R_S}$$

- Comparing the above three equations, with their counterparts without R_S indicates that including R_S results in a gain reduction by the factor $(1 + g_m R_S)$. This factor is called the amount of feedback and that it determines both the magnitude of performance improvements and, the reduction in gain.
- A resistance R_S in the source lead increases dc bias stability; that is, R_S reduces the variability in I_D. The action of R_S that reduces the variability of I_D.Rs in the circuit of Fig. 1.3 is reducing i_d. Because of its action in reducing the gain, R_S is called source degeneration resistance.
- Another useful interpretation of the voltage gain expression is that the gain from gate to drain is simply the ratio of the total resistance in the drain, (R_D in parallel with R_L), to the total resistance in the source, $[(1/g_m) + Rs]$.

1.2 BJT Amplifiers

- There are three basic configurations for single-stage BJT amplifiers:
  - Common-Emitter
  - Common-Base
  - Common-Collector

1.2.1 The basic structure of BJT amplifier

- The basic circuit that utilize to implement the various configurations of BJT amplifiers with constant current biasing is shown in figure 1.4. The value of R_B is selected as large value in order to keep the input resistance at the base large. However it is also required to limit the dc voltage drop across R_B

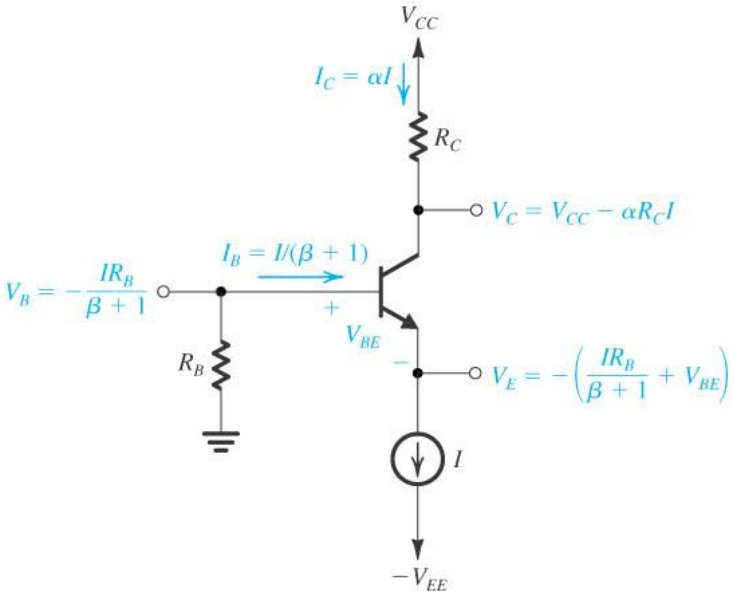
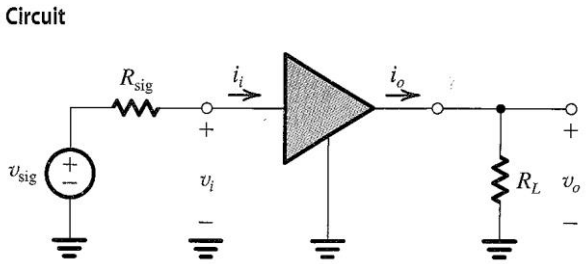


Fig. 1.4: Basic structure of the circuit used to realize single-stage, discrete-circuit BJT amplifier configurations

1.2.2 Characterizing BJT amplifiers

- To use BJT amplifier circuits, it is important to know how to characterize the performance of amplifiers as circuit building blocks. These amplifiers have internal feedback that may cause their input resistance to depend on the load resistance. Similarly internal feedback may cause the output resistance to depend on the value of the resistance of the signal source feeding the amplifier.



Definitions

- Input resistance with no load:

$$R_i \equiv \left.\frac{v_i}{i_i}\right|_{R_L=\infty}$$

- Input resistance:

$$R_{\text{in}} \equiv \frac{v_i}{i_i}$$

- Open-circuit voltage gain:

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$

- Voltage gain:

$$A_v \equiv \frac{v_o}{v_i}$$

- Short-circuit current gain:

$$A_{is} \equiv \left.\frac{i_o}{i_i}\right|_{R_L=0}$$

- Current gain:

$$A_i \equiv \frac{i_o}{i_i}$$

- Short-circuit transconductance:

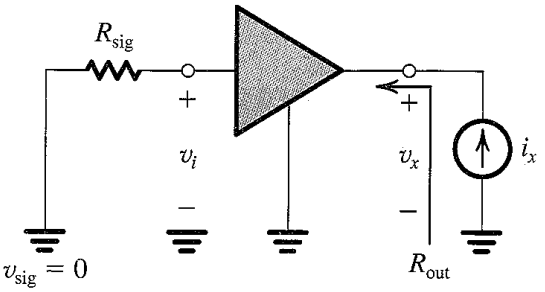
$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{R_L=0}$$

- Output resistance of amplifier proper:

$$R_o \equiv \left.\frac{v_x}{i_x}\right|_{v_i=0}$$

- Output resistance:

$$R_{\text{out}} \equiv \left.\frac{v_x}{i_x}\right|_{v_{\text{sig}}=0}$$



- Open-circuit overall voltage gain:

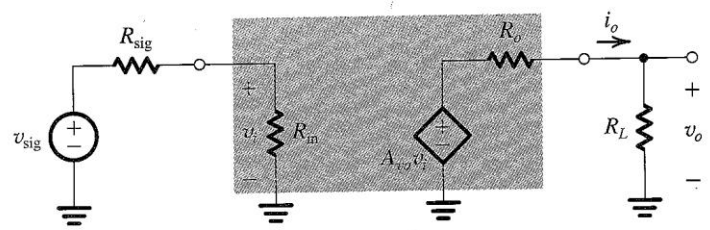
$$G_{vo} \equiv \left.\frac{v_o}{v_{\text{sig}}}\right|_{R_L=\infty}$$

- Overall voltage gain:

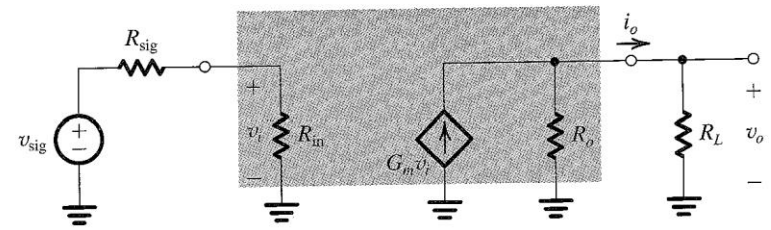
$$G_v \equiv \frac{v_o}{v_{\text{sig}}}$$

Equivalent Circuits

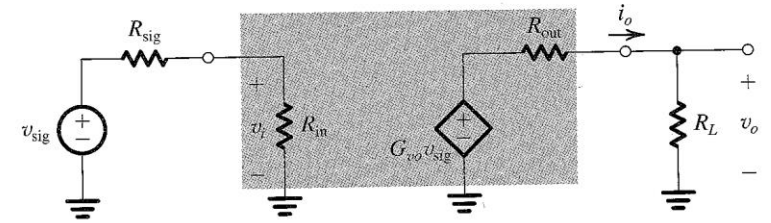
- A:



- B:



- C:



Relationships

- $\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}}$
- $A_v = A_{vo}\frac{R_L}{R_L + R_o}$
- $A_{vo} = G_m R_o$
- $G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_{vo} \frac{R_L}{R_L + R_o}$
- $G_{vo} = \frac{R_i}{R_i + R_{sig}} A_{vo}$
- $G_v = G_{vo} \frac{R_L}{R_L + R_{out}}$

1. The amplifier should fed with a signal source having an open circuit voltage v_{sig} and an internal resistance R_{sig}. These can be the parameters of an actual signal source or the Thevenin equivalent of the output circuit of another amplifier stage in a cascade amplifier stage. Similarly, R_L be the actual load resistance or the input resistance of a succeeding stage in a cascading amplifier.
2. Parameters R_i, R_o, A_{vo}, A_{is} and G_m pertain to the amplifier proper; i.e., they do not depend on the values of R_{sig} and R_L. R_{in}, R_{out}, A_v, A_i, G_{vo} and G_v may depend on the values of R_{sig} and R_L. Relationships of related pairs: $R_i = R_{in}|R_L=\infty$ and $R_o = R_{out}|R_{sig}=0$
3. For non-unilateral amplifiers, R_{in} may depends on R_L and R_{out} depends on R_{sig}. No such dependencies exists for unilateral amplifiers, for which $R_{in} = R_i$ and $R_{out} = R_o$

4. The *loading* of the amplifier on the signal source is determined by the input resistance R_{in}. The value of R_{in} determines the current that the amplifier draws from the signal source. It also determines the proportion of the signal v_{sig} that appears at the input of the amplifier proper, that is, v_i.
5. When evaluating the gain A_v from the open-circuit value A_{vo}, R_0 is the output resistance to use. This is because A_v, is based on feeding the amplifier with an ideal voltage signal v_i.

   On the other hand, if we are evaluating the overall voltage gain G_v from its open-circuit value G_{v0} the output resistance to use is R_{out} . This is because G_v is based on feeding the amplifier with v_{sig}, which has an internal resistance v_{sig} .

1.2.3 Low – frequency response of the Common-Emitter Amplifier

- First, assume Re= 0 (this is not re, but an explicit resistor)
  - The BJT is biased with a current source (with high output impedance) and a capacitor connects the emitter to ground.Capacitor provides an AC short at the emitter for small time-varying signals but is an open circuit for DC signals
- Can redraw the circuit with an equivalent circuit that replaces the BJT with its hybrid-π model

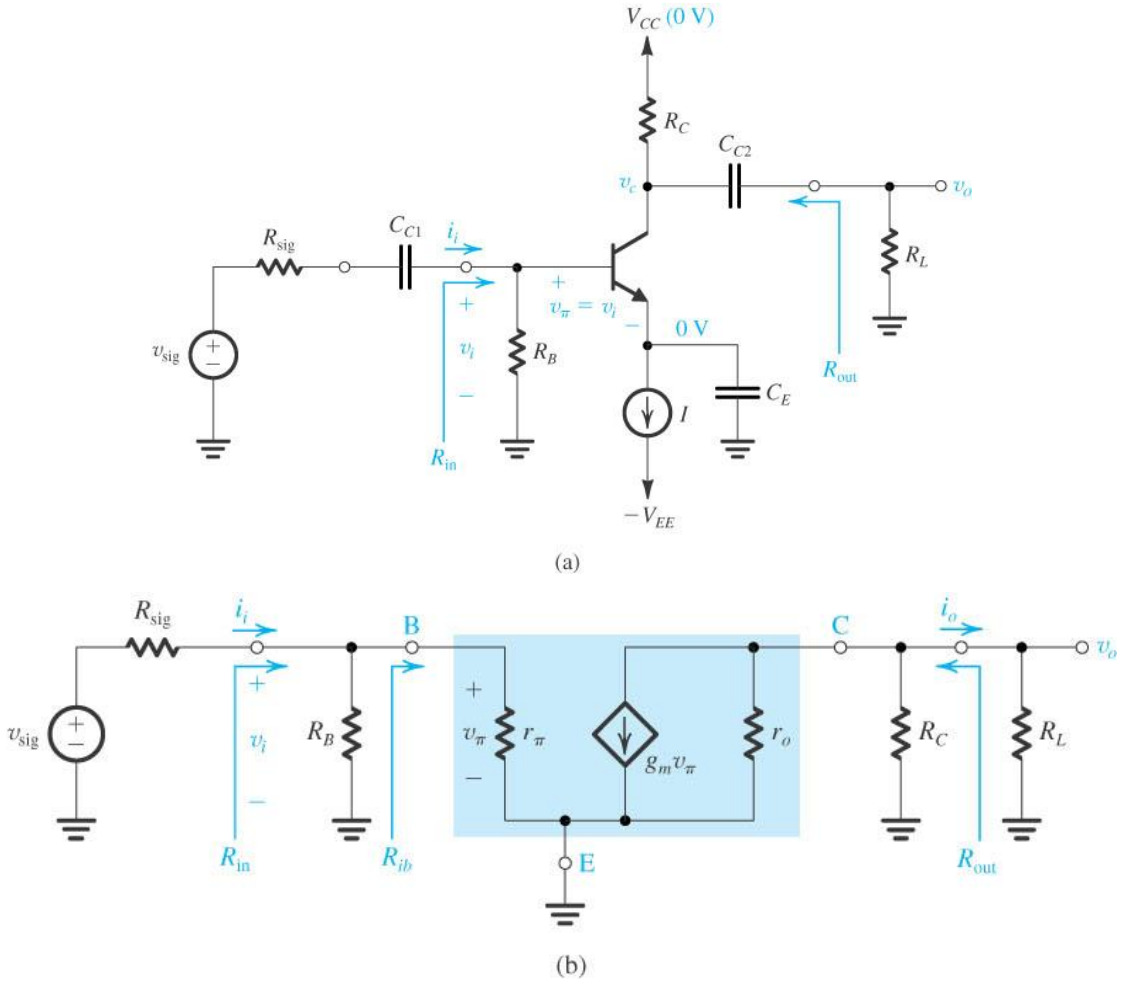


Fig. 1.5: a) CE Amplifier, b) Equivalent circuit by replacing BJT with π-model

- The terminal characteristics of amplifier are analysed as

$$R_{\text{in}} \equiv \frac{v_i}{i_i} = R_B \parallel R_{ib}$$

where R_{ib} is the input resistance looking into the base. Since the emitter is grounded,

$$R_{ib} = r_\pi$$

Normally we select $R_B >> r_\pi$, which results $R_{\text{in}} \equiv r_\pi$

- The fraction of source signal will appear across the input terminals of the amplifier and is given by,

$$v_i = v_{\text{sig}} \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}}$$

$$= v_{\text{sig}} \frac{(R_B \parallel r_\pi)}{(R_B + r_\pi) + R_{\text{sig}}}$$

which for $R_B \gg r_\pi$ becomes

$$v_i \cong v_{\text{sig}} \frac{r_\pi}{r_\pi + R_{\text{sig}}}$$

Next we note that

$$v_\pi = v_i$$

At the output of the amplifier we have

$$v_o = -g_m v_\pi (r_o \parallel R_C \parallel R_L)$$

- The voltage gain of the amplifier is

$$A_v = -g_m (r_o \parallel R_C \parallel R_L)$$

- The open circuit voltage gain is obtained by making $R_L = \infty$

$$A_{vo} = -g_m (r_o \parallel R_C)$$

from which we can say that the effect of r_0 is simply to reduce the gain, usually $r_0 >> R_C$, results in

$$A_{vo} \cong -g_m R_C$$

The output resistnace R_{out} can be found from the equivalent circuit 1.5 (b) by looking back into the output terminal while short-circuiting the source v_{sig}. This will result in $v_\pi = 0$, and

$$R_{\text{out}} = R_C \parallel r_o$$

Thus r_0 reduces the output resistance of the amplifier, typically $r_0 >> R_C$ and

$$R_{\text{out}} \cong R_C$$

For this unilateral amplifier $R_0 = R_{out}$, we can use A_{v0} and R_0 to obtain the voltage gain $A_v$corresponding to any particular R_L,

$$A_v = A_{vo}\frac{R_L}{R_L + R_o}$$

The overall voltage gain from source to load, $G_v$can be obtained by multiplying (v_i/v_{sig}) by A_v,

$$G_v = -\frac{(R_B \parallel r_\pi)}{(R_B \parallel r_\pi) + R_{\text{sig}}} g_m (r_o \parallel R_C \parallel R_L)$$

For the case $R_B >> r_\pi$, this expression simplifies to

$$G_v \cong -\frac{\beta(R_C \parallel R_L \parallel r_o)}{r_\pi + R_{\text{sig}}}$$

And voltage gain reduces to

$$G_v \cong -g_m(R_C \parallel R_L \parallel r_o)$$

- The short circuit current gain is calculated as

$$i_{os} = -g_m v_\pi$$

Since v_π is related to $i_i$by

$$v_\pi = v_i = i_i R_{\text{in}}$$

The short-circuit current gain can be found as

$$A_{is} \equiv \frac{i_{os}}{i_i} = -g_m R_{\text{in}}$$

Substituting $R_{in} = R_B \parallel r_\pi$, we can see that in the case $R_B >> r_\pi$, $|A_{is}|$ reduces to β, which is to be expected since β is the short – circuit current gain of the common – emitter configuration.

Conclusion:the common emitter configuration can provide large voltage gain, large current gain, low input resistance and relatively high output resistance.

1.2.4 Common Emitter Amplifier with Emitter Resistance

Characteristics with R_e

- gain is less with but less dependent on β
- input resistance is higher
- allows higher input signal voltage

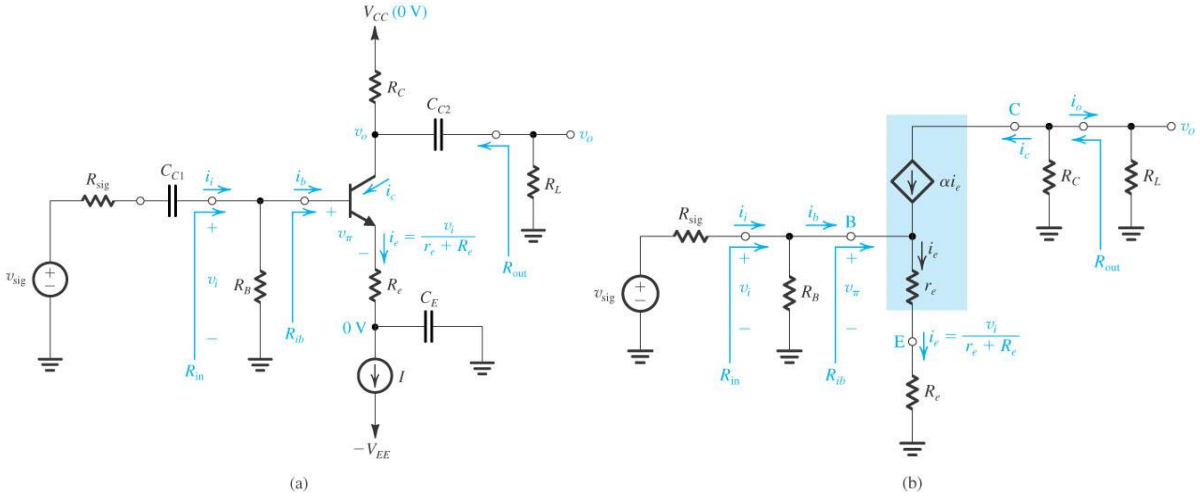


Fig. 1.6: a) CE Amplifier with emitter resistor, b) Equivalent circuit by replacing BJT with T-model

T determine the amplifier input resistance R_{in}, form the equivalent circuit shown in figure 1.6 (b), at the input R_{in} is the parallel equivalent of R_B and the input resistance at the base R_{ib}.

$$R_{\text{in}} = R_B \parallel R_{ib}$$

The input resistance at the base R_{ib} can be found from

$$R_{ib} \equiv \frac{v_i}{i_b}$$

where

$$i_b = (1-\alpha)i_e = \frac{i_e}{\beta+1}$$

and

$$i_e = \frac{v_i}{r_e + R_e}$$

Thus,

$$R_{ib} = (\beta+1)(r_e + R_e)$$

It says that the input resistance looking into the base is (1+β) times the total resistance in the emitter. Multiplication by the factor (1+β) is known as resistance – reflection rule.

$$\frac{R_{ib}\,(\text{with } R_e \text{ included})}{R_{ib}\,(\text{without } R_e)} = \frac{(\beta+1)(r_e+R_e)}{(\beta+1)r_e}$$

$$= 1 + \frac{R_e}{r_e} \cong 1 + g_m R_e$$

To determine the voltage gain A_v,

$$v_o = -i_c(R_C \parallel R_L)$$

$$= -\alpha i_e(R_C \parallel R_L)$$

$$A_v \equiv \frac{v_o}{v_i} = -\frac{\alpha(R_C \parallel R_L)}{r_e + R_e}$$

Since $\alpha \cong 1$,

$$A_v \cong -\frac{R_C \parallel R_L}{r_e + R_e}$$

The open circuit voltage gain is given by

$$A_{vo} = -\frac{\alpha R_C}{r_e + R_e}$$

which can be expressed alternatively as

$$A_{vo} = -\frac{\alpha}{r_e}\frac{R_C}{1 + R_e/r_e}$$

$$A_{vo} = -\frac{g_m R_C}{1 + (R_e/r_e)} \cong -\frac{g_m R_C}{1 + g_m R_e}$$

Including R_e thus reduces the voltage gain by the factor $(1+g_mR_e)$, which is the same factor by which R_{ib} is increased.

The output resistance R_{out} can be found from the circuit, $R_{out} = R_C$.

The short – circuit current gain A_{is} can be found from the circuit

$$i_{os} = -\alpha i_e$$

$$i_i = v_i / R_{in}$$

$$A_{is} = -\frac{\alpha R_{in} i_e}{v_i}$$

$$A_{is} = -\frac{\alpha(R_B \parallel R_{ib})}{r_e + R_e}$$

which for the case $R_B \gg R_{ib}$ reduces to

$$A_{is} = \frac{-\alpha(\beta+1)(r_e+R_e)}{r_e+R_e} = -\beta$$

the same value as for the CE circuit.

The overall voltage gain from source to load can be obtained by multiplying A_v by (v_i/v_{sig})

$$G_v = \frac{v_i}{v_{sig}} \cdot A_v = -\frac{R_{in}}{R_{sig}+R_{in}} \frac{\alpha(R_C \parallel R_L)}{r_e+R_e}$$

Substituting for R_{in} by $R_B \parallel R_{ib}$, assuming that $R_B \gg R_{ib}$, and substituting for R_{ib}

$$G_v \cong -\frac{\beta(R_C \parallel R_L)}{R_{sig}+(\beta+1)(r_e+R_e)}$$

This gain is lower than that of the CE amplifier because of the additional term (1+ β) R_e in the denominator.

$$\frac{v_\pi}{v_i} = \frac{r_e}{r_e+R_e} \cong \frac{1}{1+g_m R_e}$$

Thus, for the same v_π, the signal at the input terminal of the amplifier, v_i, can be greater than for the CE amplifier by the factor ($1+g_mR_e$).

Conclusion:

- The input resistance R_{ib} is increased by the factor ($1+g_mR_e$).
- The voltage gain from base to collector, A_v is reduced by the factor ($1+g_mR_e$).
- For the same nonlinear distortion, the input signal v_i can be increased by the factor ($1+g_mR_e$).
- The overall voltage gain is less dependent on the value of β.
- The high – frequency response is significantly improved.

UNIT-I

Assignment-Cum-Tutorial Questions

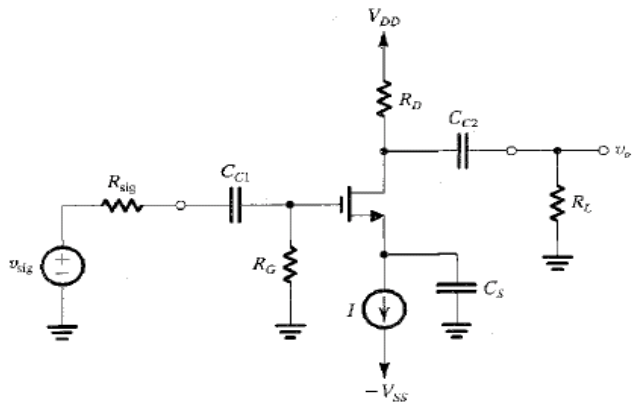
A. Objective Questions

1. Which of the following is true in case of unilateral amplifiers [ ]
   a) Input resistance doesn't depend on R_L
   b) Output resistance doesn't depend on R_{sig}
   c) Both a & b
   d) None of the above.
2. All practical amplifiers are [ ]
   a) Unilateral b) Non-unilateral
   c) May be sometimes unilateral d)None
3. The phase difference between the output and input voltages of a CE amplifier is ..... [ ]
   a) 180^o b) 0^o c) 90^o d) 270^o
4. The purpose of capacitors in a transistor amplifier is to ..... [ ]
   a) Protect the transistor b) Cool the transistor
   b) Couple or bypass a.c. component d)Provide biasing
5. If the input capacitor of a transistor amplifier is short-circuited, then..... [ ]
   a) Transistor will be destroyed b) Biasing conditions will change
   c)Signal will not reach the base d) None of the above
6. The amplifier works as a linear system for ..... [ ]
   a) High frequency signals b) Low frequency signals
   c)Small signals d) large signals
7. State the differences between Unilateral and Non Unilateral Amplifiers
8. Draw the CS Amplifier and its equivalent circuit for small- signal analysis.
9. Draw the CS Amplifier with source resistance and its equivalent circuit for small- signal analysis
10. Why Source Resistance in CS amplifier also called as "Source degeneration" resistance.
11. Define Bandwidth and Figure of Merit of an amplifier?
12. Draw the basic structure of the circuit used to realize single-stage discrete-circuit BJT amplifier configurations.
13. Draw the frequency response curve of an amplifier?

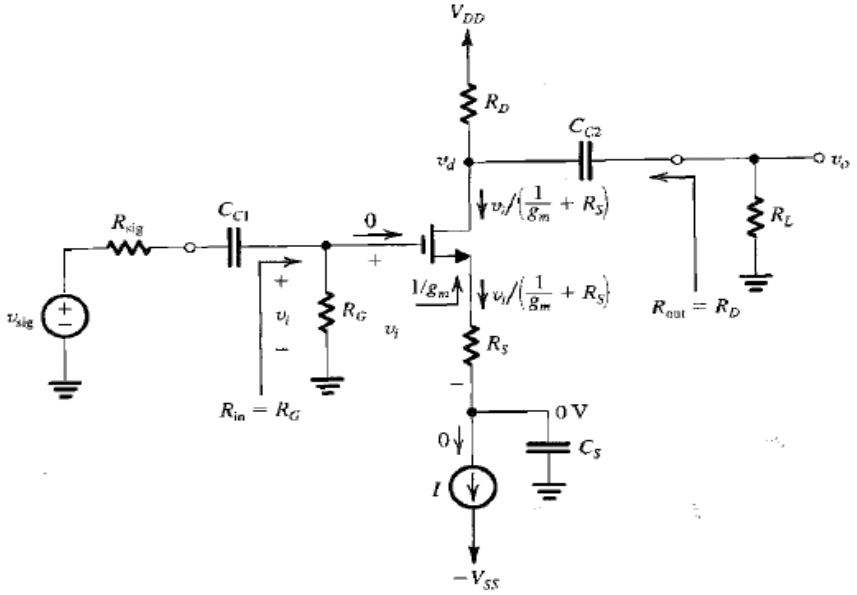
14. Draw the basic structure of the circuit used to realize single-stage discrete-circuit MOS amplifier configurations.

B.Subjective Questions

1. What are the characteristic parameters of amplifiers? Define & provide relationships.
2. Explain the Small signal operation of CS amplifier. Find the expressions for input resistance (R_{in}), Output resistance (R_{out}), voltage gain (A_v) and overall voltage gain(G_v).
3. Analyse the CS amplifier with source degeneration resistance to find the expressions for R_{in}, R_{out}, A_v and G_v.
4. Analyse the CE amplifier with emitter degeneration resistance to find the expressions for R_{in}, Rout, A_v ,i_{os} and G_v.
5. Explain the small signal operation of CE amplifier & deduce the expressions for R_{in}, R_{out}, A_v, i_{os} and G_v.
6. Considering a CS amplifier, find R_{in}, A_{vo}, and R_{out}, both without and with r_o taken into account. Then calculate the overall voltage gain G_v, with r_o taken into account, for the case R_{sig} = 100 kΩ, R_L = 15 kΩ. If v_{sig} is a 0.4V Peak to peak sinusoid, what output signal v_o results?
7. Calculate the overall voltage gain G_v of a common source amplifier for which g_m = 2 mA/V, r_0 = 50 kΩ, R_D = 10 KΩ, and R_G = 10 MΩ. The amplifier is fed from a signal source with a Thevenin resistance of 0.5 MΩ, and the amplifier output is coupled to a load resistance of 20 KΩ.
8. A CS amplifier using an NMOS transistor biased in the manner as shown in below figure for which g_m = 2 mA/V is found to have an overall voltage gain G_0 of -16 V/V. What value should a resistance R_S inserted in the source lead have to reduce the voltage gain by a factor of 4?

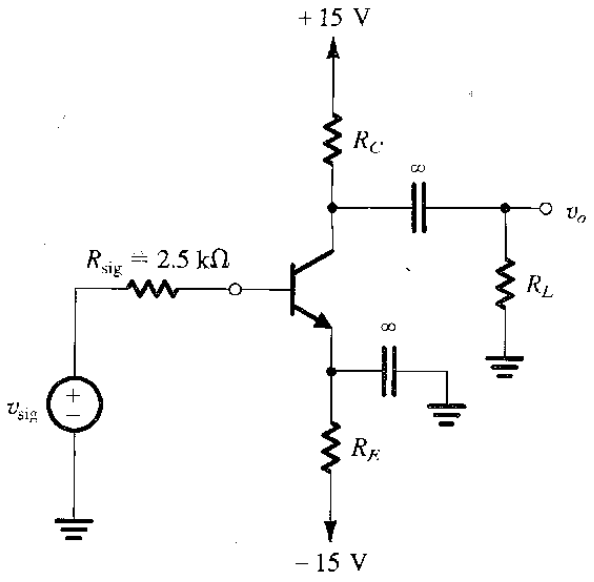


9. The overall voltage gain of the amplifier as shown in below figure was measured with a resistance R_s of 1 KΩ in place and found to be -10 V/V. When R_s is shorted, but the circuit operation remained linear the gain doubled. What must g_m be? What value of R_s is needed to obtain an overall voltage gain of-8V/V?



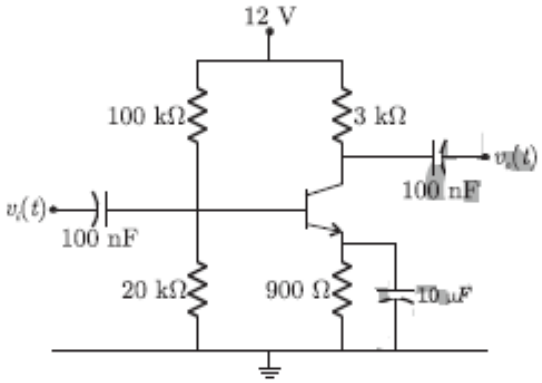
10. A BJT amplifier is measured to have R_i =10 kΩ**.** A_{v0}= 100 V/V, and R_0= 100 **Ω.** Also, when a load resistance $R_L$of 1 kΩ is connected between the output terminals, the input resistance is found to decrease to 8 kΩ. If the amplifier is fedwith a signal source having an internal resistance of 2 kΩ,
findG_m, A_v, G_{v0}, G_v, R_{out}, and A_i.

11. In the circuit shown below, v_{sig} is a small sinewavesignal with zero average. The transistor β is 100.
(a) Find the value of R_E to establish a dc emitter current ofabout 0.5 mA.
(b) Find R_C to establish a dc collector voltage of about +5 V.
(c) For R_L= 10 kΩ and the transistor r_0 = 200 kΩ, draw thesmall-signal equivalent circuit of the amplifier and determineits overall voltage gain.



C. GATE questions

1. A small signal source V_i (t) = (Acos 20t +Bsin 10 t) is applied to a transistor amplifieras shown below. The transistorhas β = 150 and h_{ie}= 3Ω. Which expression bestapproximate V_0(t)? (GATE 2009) [ ]



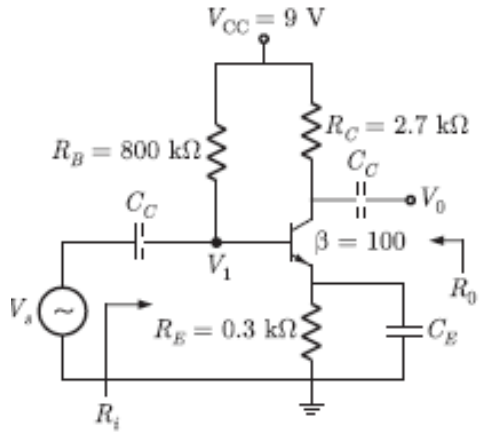
(A) V_0(t) = 1500(Acos 20t+ Bsin 10 t)

(B) V_0(t) =1500(Acos 20t + Bsin 10 t)

(C) V_0(t) = 1500Bsin 10 t

(D) V_0(t)= 150Bsin 10 t

2. The amplifier circuit shown below uses a silicon transistor. The capacitors C_C and C_E can be assumed to be short at signal frequency and effect of output Resistancer_0 can be ignored. If C_E is disconnected from the circuit, which one of the followingstatements is true? (GATE 2010) [ ]



(A) The input resistance $R_i$increases and magnitude of voltage gain$A_V$decreases

(B) The input resistance $R_i$decreases and magnitude of voltage gain A_V increases

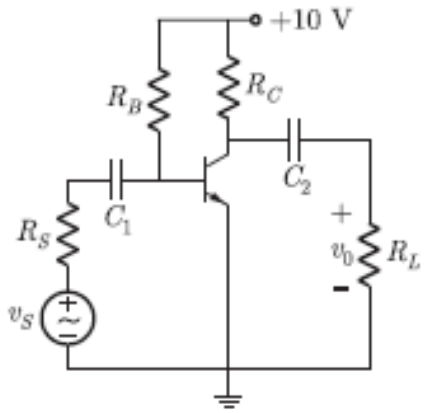
(C) Both input resistance $R_i$and magnitude of voltage gain $A_V$decreases

(D) Both input resistance $R_i$and the magnitude of voltage gain $A_V$increases

3. Consider the common emitter amplifier shown below with the following circuit

parameters:

β=100,g_m=0.3861A/V,r_0=259Ω,R_S=1kΩ,R_B=93kΩ,R_C=250kΩ,R_L=1kΩ,C_1=3μFandC_2= 4.7 μF



The resistance seen by the source v_S is .....(GATE 2010) [ ]

(A) 258 Ω (B) 1258 Ω (C) 93 kΩ (D) ∞

Unit – II

High – frequency single – stage amplifiers

Objectives

- To Discuss the General considerations of High – frequency Response of an amplifier.
- To Discuss the High-frequency response of the CS and CE amplifiers
- Analysis CS and CE of amplifiers using Miller's theorem
- To analyze, and characterize the different Cascode Amplifiers like MOS Cascode and BJT Cascode
- To analyze, and characterize the Darlington configuration.

Syllabus

General considerations, high-frequency response of CS and CE amplifiers, cascade amplifier, Darlington configuration.

Pre-requisites

- The MOSFET internal Capacitances
- The High-Frequency MOSFET Model
- The BJT Internal Capacitances and High Frequency Model
- Circuit models for amplifiers
- The terms: Frequency response and Bandwidth of an amplifier

Outcomes:

Students will be able to

Draw, analyse, and characterize the MOS and BJT single-stage amplifiers at high frequencies.

Draw, analyze, and characterize - Cascode, Darlington,

Pre-requisites

THE MOSFET INTERNAL CAPACITANCES :

There are basically two types of internal capacitances in the MOSFET

1. The gate capacitive effect: The gate electrode (polysilicon) forms a parallel-plate capacitor with the channel, with the oxide layer serving as the capacitor dielectric. W e discussed the gate (or oxide) capacitance in previous sections and denoted its value per unit area as *Cox.*

2. The source-body and drain-body depletion-layer capacitances: These are the capacitances of the reverse-biased *pn* junctions formed by the *n+* source region (also called the diffusion) and the p-type substrate and by the *n+* drain region (the drain diffusion) and the substrate.

The Junction Capacitances :

The depletion-layer capacitances of the two reverse-biased junctions formed between each of the source and the drain diffusions and the body can b e determined using the formula developed in previous Section . Thus, for the source diffusion, we have the source body capacitance, *Csb,*

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}}$$

here Csb_0 is the value of *Csb* at zero body-source bias, *VSB* is the magnitude of the reverse bias voltage, and V_0 is the junction built-in voltage (0.6V to 0.8V). Similarly, for the drain diffusion, we have the drain-body capacitance *Cdb,*

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}}$$

The High-Frequency MOSFET Model:

The below figure shows the high frequency model of MOSFET by adding all the capacitances.

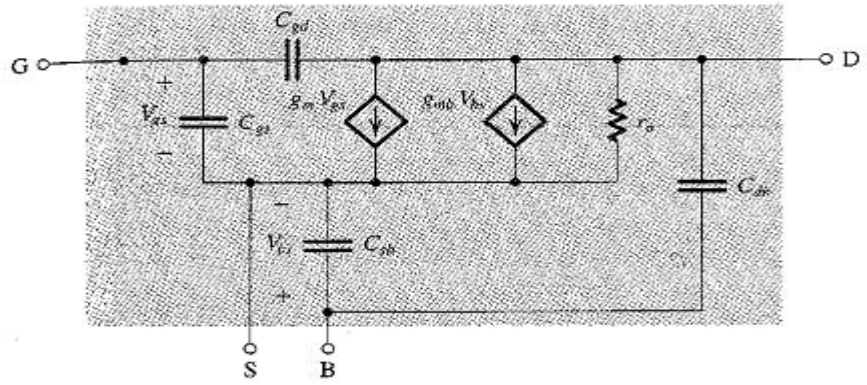


Figure 1a: High-frequency equivalent circuit model for the MOSFET.

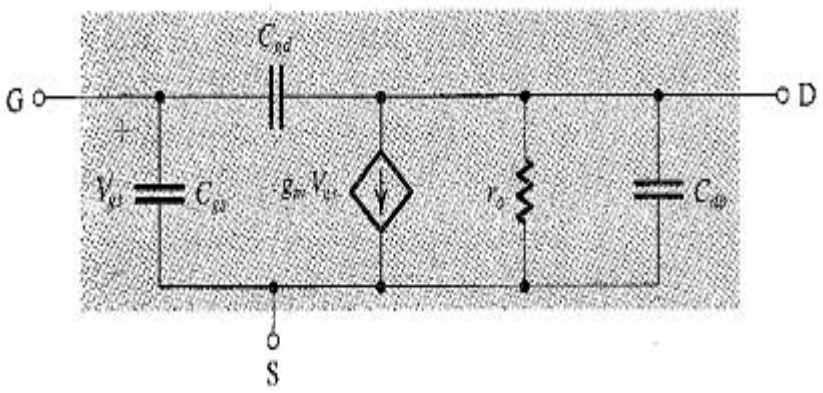


Figure 1b: The equivalent circuit for the case in which the source is connected to the substrate (body),

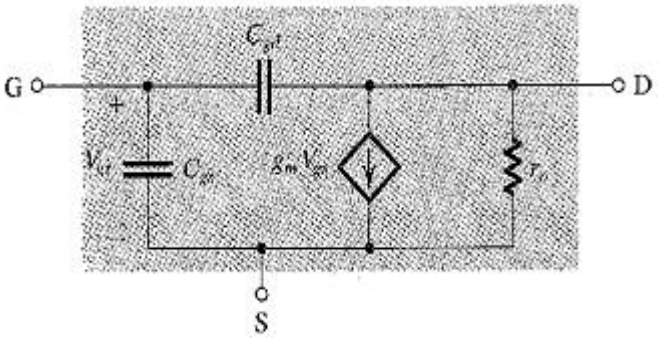


Figure 1c: The equivalent circuit model of (b) with *Cdb* neglected (to simplify analysis).

The MOSFET Unity-Gain Frequency *(f_T):*

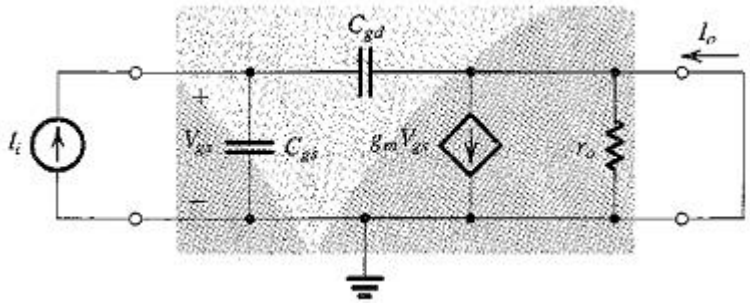


Figure 2: Circuit for determining the short-circuit current gain $I_o/1_i$.

A figure of merit for the high-frequency operation of the MOSFET as an amplifier is the unity-gain frequency, f_T. This is defined as the frequency at which the short-circuit current gain of the common-source configuration becomes unity. The above figure shows the MOSFET hybrid ∏- model with the source as the common terminal between the input and output ports. To determine the short-circuit current gain, the input is fed with a current-source signal I_i• and the output terminals are short-circuited. It is easy to see that the current in the short circuit is given by

$$I_o = g_m V_{gs} - sC_{gd}V_{gs}$$

let us assume C_{gd} is a very small value and it can be neglected

w e can express *Vgs* in terms of the input current I_i as

$$V_{gs} = I_i / s(C_{gs} + C_{gd})$$

By the above two equations we can get the short circuit current gain as

$$\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})}$$

For physical frequencies *S=JW,* it can be seen that the magnitude of the current gain becomes unity at the frequency

$$\omega_T = g_m / (C_{gs} + C_{gd})$$

Thus the unity-gain frequency f_T is given as

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Hence f_T is proportional to *gm* and inversely proportional to the FET internal capacitances.

The BJT Internal Capacitances and High Frequency Model

The high frequency response of BJT amplifiers rolls off due to short circuiting effect of internal capacitances. These internal capacitances are resulting from charge- storage effects.

The High frequency Hybrid- π model is shown as below.

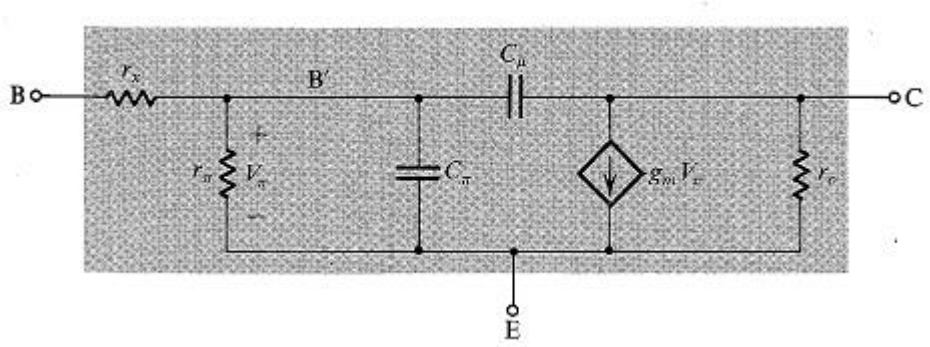


Fig. The High- Frequency Hybrid - π model

r_x : Base Spreading Resistance :

It is the resistance between the external base terminal B and internal node B' (also called as implicit node, bulk node). Its typical value is 100Ω. negligible at low frequencies but effective at high frequencies.

r_Π: It is the resistnace looking into the base terminal.

typical value is 1KΩ.

There are two sources of internal capacitances effect

1. Base- Emitter Capacitance Cπ

2. Collector –Base Junction Capacitance Cμ

1. Base- Emitter Capacitance Cπ :

Cπ is the sum of two capacitances .Cde Emitter- Base Diffusion Capacitance

Cje Emitter – Base Junction Capacitance.

$$C\pi = Cde + Cje$$

i) Cde Emitter- Base Diffusion Capacitance: It is called as Base – Charging or Diffusion Capacitance Cde.

It is due to minority carrier storage in the base region when the transistor is operating in the active or satuaration mode. i.e when Emitter- Base Junction (EBJ) is forward biased.

$Cde = dQ/dv_{BE}$

considering , an npn transistor in active region..

$$i_C = I_S e^{v_{BE}/V_T} \quad \text{.....(1)}$$

$$I_S = \frac{A_E q D_n n_i^2}{N_A W} \quad \text{……(2)}$$

$$Q_n = \frac{A_E q W n_i^2}{2N_A} e^{v_{BE}/V_T} \quad \text{…….(3)}$$

Using 1, 2, 3

$$Q_n = \frac{W^2}{2D_n} i_C = \tau_F i_C$$

where, $$\tau_F = \frac{W^2}{2D_n}$$

τ_F is known as the forward base- transit time. It represents the average time a charge carrier (electron) spends in crossing the base.

$$C_{de} \equiv \frac{dQ_n}{dv_{BE}}$$

$$= \tau_F \frac{di_C}{dv_{BE}}$$

$$C_{de} = \tau_F g_m = \tau_F \frac{I_C}{V_T}$$

ii :Cje :: Base – Emitter Junction Capacitance

$$C_{je} = \frac{C_{je0}}{\left(1 - \frac{V_{BE}}{V_{0e}}\right)^m}$$

Where, Cje0 is the value of Cjeat VBE = 0V.

V_{0e} is the EBJ built in voltage (0.7 – 0.9 V)

m = grading coefficient , typically ½.

For a forward biased EBJ in the active mode, Cje = 2 Cje0

Typical value of Cπ is 100pF.

2. The Collector – Base Junction Capacitance Cμ

This is the capacitance of the reverse biased Collector – Base Junction (CBJ) .

$$C_\mu = \frac{C_{\mu 0}}{\left(1 + \frac{V_{CB}}{V_{0c}}\right)^m}$$

where Cμ0 is the value of Cμ at VCB = 0V.

Voc is the CBJ built in voltage (typically 0.75 V)

m is grading coeffiecient = 1/2 to 1/3 .

Typical value of Cμ= 3pF.

Unity Gain Frequency (F_T)

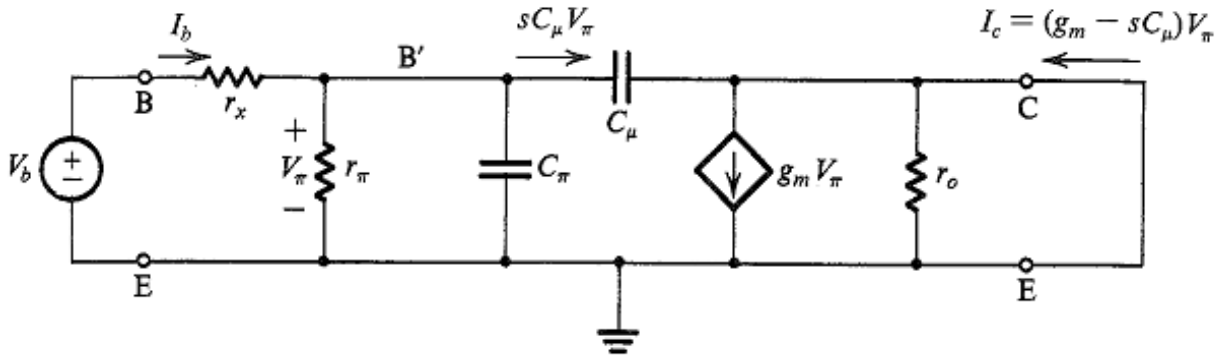


Fig. The Circuit for deriving an expression for Short Circuit current gain $h_{fe}(s)$ = Ic/ Ib.

$$I_c = (g_m - sC_\mu)V_\pi \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$V_\pi = I_b(r_\pi // C_\pi // C_\mu) = \frac{I_b}{1/r_\pi + sC_\pi + sC_\mu} \quad \ldots\ldots\ldots\ldots (2)$$

$$h_{fe} \equiv \frac{I_c}{I_b} = \frac{g_m - sC_\mu}{1/r_\pi + s(C_\pi + C_\mu)} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Since, $g_m \gg \omega C_\mu$;

$$h_{fe} \simeq \frac{g_m r_\pi}{1 + s(C_\pi + C_\mu)r_\pi}$$

$$h_{fe} = \frac{\beta_0}{1 + s(C_\pi + C_\mu)r_\pi}$$

Where β_0 is the low frequency value of β

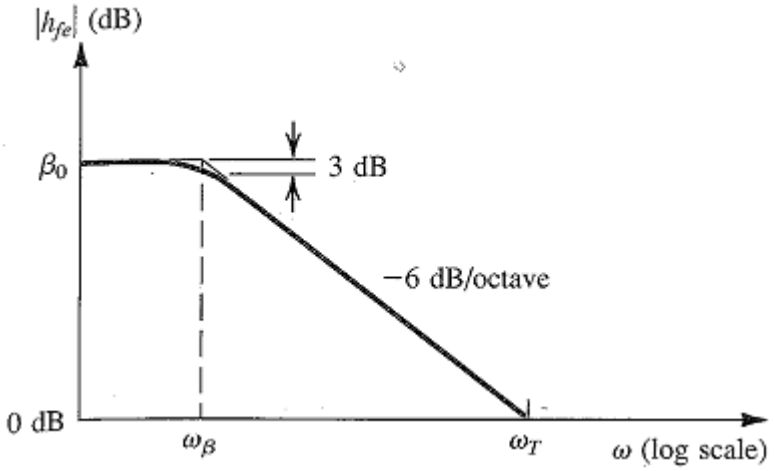


Fig. Frequency Response of h_{fe}

f_β is the 3-dB frequency

$$\omega_\beta = \frac{1}{(C_\pi + C_\mu) r_\pi}$$

The unity gain frequency is given by

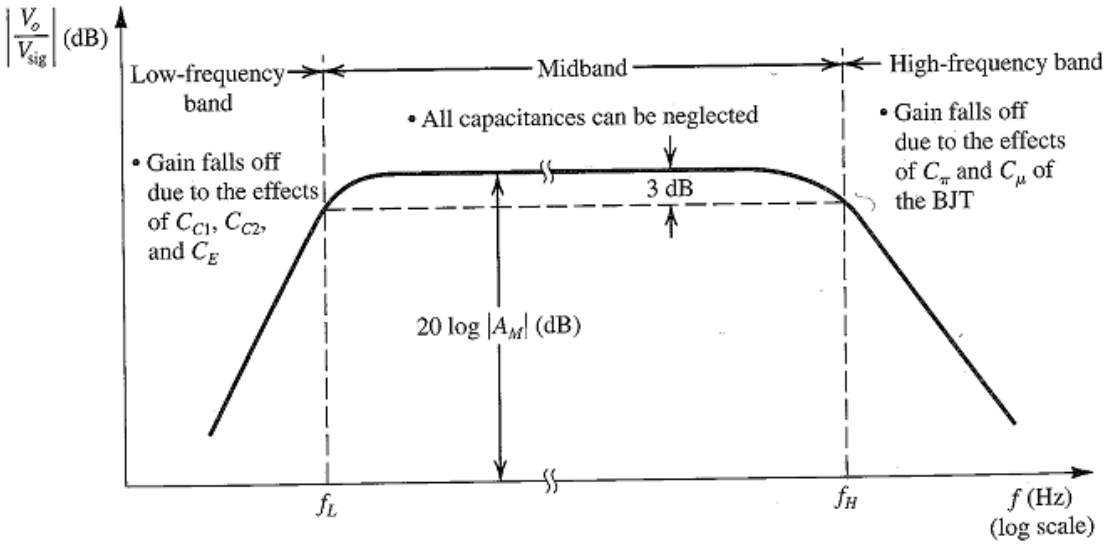
$$\omega_T = \beta_0 \omega_\beta$$

Thus

$$\omega_T = \frac{g_m}{C_\pi + C_\mu}$$

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

Frequency Response of CE Amplifier:



Low frequency Band: The gain roll off in this region is due to coupling and bypass capacitors acting as open circuit & internal capacitances are open and in significant.

Mid frequency Band: In this region coupling and bypass capacitors will be short circuited; where as the internal capacitances are open circuits and still in effective. Hence the gain is maximum and almost constant.

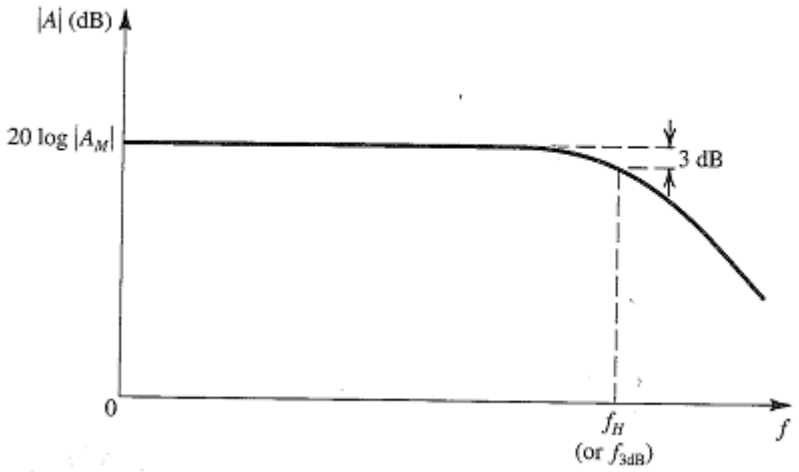
High frequency Band: The gain roll off in this region is due to internal capacitances getting slowly short circuiting.

SYLLABUS

2.1 High Frequency Response – General Consideration**,** The high-frequency gain function, Determining the 3-dB frequency $f_{H,}$ Using open-circuit time constants for the approximate determination of $f_{H,}$

2.1.1 General Consideration

The various stages in an integrated- circuit cascade amplifier are directly coupled; that is they do not utilize coupling capacitors. Hence the mid band gain remains constant down to zero frequency.



2.1.2 The High- Frequency Gain Function:

The amplifier gain, taking into account the internal transistor capacitances, can be expressed as a function of the complex frequency variable s in the general form

$$A(s) = A_M F_H(S)$$

where A_M is the midband gain.

Considering the generalized transfer function

$$F_H(s) = \frac{(1+s/\omega_{Z1})(1+s/\omega_{Z2})\ldots(1+s/\omega_{Zn})}{(1+s/\omega_{P1})(1+s/\omega_{P2})\ldots(1+s/\omega_{Pn})}$$

where wp1, wp2, …. wpn are pole frequencies.

wz1, wz2,…. 2zn are zero frequencies.

2.1.3 Determining the 3-dB frequency f_H:

i) Dominant pole is present:

The amplifier designer usually is particularly interested in the part of the high-frequencyband that is close to the midband. This is because the designer needs to estimate-and ifneed be modify-the value of the upper 3-dB frequency f_H. In many cases the zeros are either at infinity or suchhigh frequencies as to be of little signiicance to the determination of a)H.

If in addition oneof the poles, says w_{Pl}, is of much lower frequency than any of the other poles, then this polewill have the greatest effect on the value of the amplifier w_H. In other words, this pole willdominate the high-frequency response of the amplifier, and the amplifier is said to have **adominant-pole response**. In such cases the function $F_H(s)$ can be approximated by

$$F_H(s) \cong \frac{1}{1+s/\omega_{P1}}$$

If a dominant pole exists, then the determination of W_H is greatly simplified

$$\boxed{\omega_H \cong \omega_{P1}}$$

This approximation is valid only when the **Dominant pole** is existing.

A **Dominant pole** is said to be existing iff the lowest frequency pole is at least two octaves (a factor of 4) lowest from nearest pole or zero.

ii) Dominant pole not existing

If a dominant pole does not exist, the 3-dB frequency W_H can be determined alternatively, by an approximate formula for w_H, that can be derived as follows:

Consider,for simplicity, the case of a circuit having two poles and two zeros in the high-frequency

Band; that is

$$F_H(s) = \frac{(1 + s/\omega_{Z1})(1 + \bar{s}/\omega_{Z2})}{(1 + s/\omega_{P1})(1 + s/\omega_{P2})}$$

Substituting $s = j\omega$ and taking the squared magnitude gives

$$|F_H(j\omega)|^2 = \frac{(1 + \omega^2/\omega_{Z1}^2)(1 + \omega^2/\omega_{Z2}^2)}{(1 + \omega^2/\omega_{P1}^2)(1 + \omega^2/\omega_{P2}^2)}$$

By definition, at $\omega = \omega_H$, $|F_H|^2 = \frac{1}{2}$; thus,

$$\frac{1}{2} = \frac{(1 + \omega_H^2/\omega_{Z1}^2)(1 + \omega_H^2/\omega_{Z2}^2)}{(1 + \omega_H^2/\omega_{P1}^2)(1 + \omega_H^2/\omega_{P2}^2)}$$

$$= \frac{1 + \omega_H^2\left(\frac{1}{\omega_{Z1}^2} + \frac{1}{\omega_{Z2}^2}\right) + \omega_H^4/\omega_{Z1}^2\omega_{Z2}^2}{1 + \omega_H^2\left(\frac{1}{\omega_{P1}^2} + \frac{1}{\omega_{P2}^2}\right) + \omega_H^4/\omega_{P1}^2\omega_{P2}^2}$$

Since w_H is usually smaller than the frequencies of all the poles and zeros, So by neglecting the terms containing fourth order $w_H$terms.

$$\omega_H \cong 1\Big/\sqrt{\frac{1}{\omega_{P1}^2} + \frac{1}{\omega_{P2}^2} - \frac{2}{\omega_{Z1}^2} - \frac{2}{\omega_{Z2}^2}}$$

This relationship can be extended to any number of poles and zeros as

$$\omega_H \cong 1\Big/\sqrt{\left(\frac{1}{\omega_{P1}^2} + \frac{1}{\omega_{P2}^2} + \cdots\right) - 2\left(\frac{1}{\omega_{Z1}^2} + \frac{1}{\omega_{Z2}^2} + \cdots\right)}$$

iii) Using Open Circuit Time Constants for the Approximate Determination of f_H

it is not a simple matterto determine the poles and zeros by quick hand analysis. In such cases an approximate value for f_H can be obtained using this method.

Considering the generalized transfer function

$$F_H(s) = \frac{(1 + s/\omega_{Z1})(1 + s/\omega_{Z2})\ldots(1 + s/\omega_{Zn})}{(1 + s/\omega_{P1})(1 + s/\omega_{P2})\ldots(1 + s/\omega_{Pn})}$$

$$F_H(s) = \frac{1 + a_1 s + a_2 s^2 + \cdots + a_n s^n}{1 + b_1 s + b_2 s^2 + \cdots + b_n s^n}$$

where the coefficients ***a*** and ***b*** are related to the frequencies of the zeros and poles, respec-tively. Specifically, the coefficient ***b1*** is given by

$$b_1 = \frac{1}{\omega_{P1}} + \frac{1}{\omega_{P2}} + \cdots + \frac{1}{\omega_{Pn}} \quad \ldots\ldots\ldots\ldots\ldots\ldots(1)$$

The value of ***b1*** can be obtained by considering the various capacitances in the high-frequency equivalent circuit one at a time whilereducing all other capacitors to zero (or, equivalently, replacing them with open circuits). That is, to obtain the contribution of capacitance C, we reduce all other capacitances to zero, reduce input signal source to zero and determine the resistance Rio seen by Ci.

This process is repeated for all other capacitors in the circuit. The value of b1 is computed by summing the individual time constants, hence called Open – Circuit Time Constants.

$$b_1 = \sum_{i=1}^{n} C_i R_{io}$$

Now the approximate value of $f_H$can be obtained by considering there exist a dominant pole w_{P1} then

from eq.(1)

$$b_1 \simeq \frac{1}{\omega_{P1}}$$

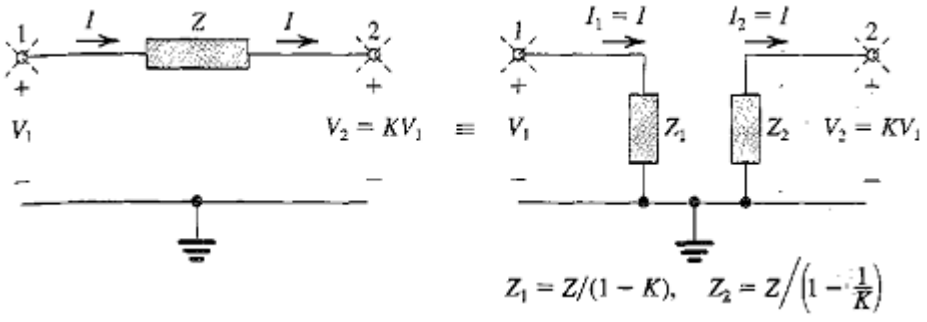
But also upper 3dB frequency will be approximately equal to w_{p1}leading to the approximation

$$\omega_H \simeq \frac{1}{b_1} = \frac{1}{[\sum_i C_i R_{io}]}$$

2.2 MILLERS THEORM:

Consider the situation in Figure 5a As a part of a larger circuit that is not shown, we have isolated two circuit nodes, labeled 1 and 2, between which an impedance Z is connected. Nodes 1 and 2 are also connected to other parts of the circuit, as signified by the broken lines emanating from the two nodes. Furthermore, it is assumed that somehow it has been determined that the node voltage at node 2 is related to the node 1 by

$$V_2 = K\, V_1$$



The Miller equivalent circuit.

In typical situations *K is* a gain factor that can be positive or negative and that has a magnitude usually larger than unity. This, however, is not an assumption for Miller's theorem. Miller's theorem states that impedance Z can be replaced by two impedances: Z1 connected between node 1 and ground and Z2 connected between node 2 and ground, where

$$Z_1 = Z/(1-K)$$

and

$$Z_2 = Z\Big/\left(1-\frac{1}{K}\right)$$

The current entering in to node1 is given as below

$$I_1 = \frac{V_1}{Z_1} = I = \left(\frac{V_1 - KV_1}{Z}\right)$$

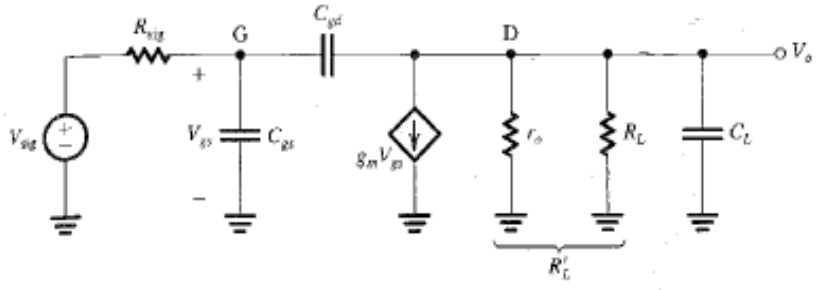
similarly current entering into node2 is given as below

$$I_2 = \frac{0-V_2}{Z_2} = \frac{0-KV_1}{Z_2} = I = \frac{V_1 - KV_1}{Z}$$

Although not highlighted, the Miller equivalent circuit derived above is valid only as long as the rest of the circuit remains unchanged; otherwise the ratio of ,V2 to V1 might change. It follows that the Miller equivalent circuit cannot be used directly to determine the output resistance of an amplifier. This is because in determining output resistances it is implicitly assumed that the source signal is reduced to zero and that a test-signal source (voltage or current) is applied to the output terminals—obviously a major change in the circuit, rendering the Miller equivalent circuit no longer valid.

2.3 High-frequency response of the CS and CE amplifiers : High-frequency response of the CS and CE amplifiers, Analysis using Miller's theorem, Analysis using open-circuit time constants, Exact analysis, Adapting the formulas for the case of the CE amplifier, The situation when R_{sig} is low

2.3 High-frequency response of the CS and CE amplifiers:



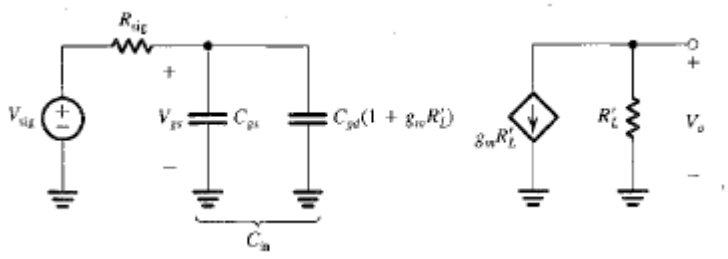
The above figure shows the High-frequency response equivalent circuit of the common source amplifier. This equivalent circuit applies equally well to the CE amplifier while a simple relabeling of components Cgs would be replaced by C*π*, Cgd by Cμ and obviously *Vgs by vπ.*

The input-signal source is represented by Vsig and *Rsig.* In some cases, however, Vsig and *Rsig* would be modified values of the signal-source voltage and internal resistance, taking into account other resistive components such as a bias resistor R_G or R_B, the BJT resistances *rx* and *rπ*, etc. The load

resistance *RL* represents the combination of an actual load resistance (if one is connected) and the output resistance of the current-source load. To avoid loss of gain, R_L is usually on the same order as r_0. We combine R_L with r_a and denote their parallel equivalent R_L'. The load capacitance C_L represents the total capacitance between drain (or collector) and ground; it includes the drain-to-body capacitance *Cdb* (collector-to-substrate capacitance), the input capacitance of a succeeding amplifier stage, and in some cases, as we shall see in later chapters, a deliberately introduced capacitance. In IC MOS amplifiers, C_L can be relatively substantial.

2.3.1 Analysis Using Miller's Theorem

In situations when *Rsig* is relatively large and C_L is relatively small, Miller's theorem can be used to obtain a quick but approximate estimate of the 3-dB frequency f_H. Below fig shows the approximate equivalent circuit obtained for the CS case, from which we see that the amplifier has a dominant pole formed



by R_{sig} and C_{in}. Thus,

$$\frac{V_o}{V_{sig}} \cong \frac{A_M}{1 + \frac{s}{\omega_H}}$$

where

$$A_M = -g_m R_L'$$

and the 3-dB frequency $f_H = \omega_H / 2\pi$ is given by

$$f_H = \frac{1}{2\pi C_{in} R_{sig}}$$

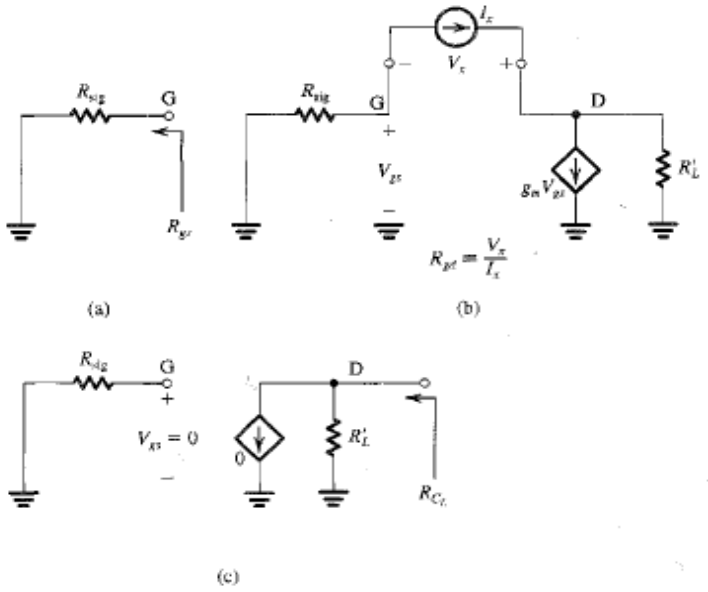
where

$$C_{in} = C_{gs} + C_{gd}(1 + g_m R_L')$$

2.3.2 Analysis Using Open-Circuit Time Constants

The method of open-circuit time constants can b e directly applied to the CS equivalent circuit of from which we see that the resistance seen by *Cgs, Rgs = Rsig* and that seen by C_L is R'_L. The resistance *R d* seen by *Cgd* can b e found by analyzing the circuit.

$$R_{gd} = R_{sig}(1 + g_m R_L') + R_L' \quad ($$



Thus the effective time-constant b_1 or τ_H can be found as

$$\begin{aligned}\tau_H &= C_{gs}R_{gs} + C_{gd}R_{gd} + C_L R_{C_L} \\ &= C_{gs}R_{sig} + C_{gd}[R_{sig}(1 + g_m R_L') + R_L'] + C_L R_L'\end{aligned}$$

and the 3-dB frequency f_H is

$$f_H \cong \frac{1}{2\pi\tau_H}$$

2.3.3 Exact Analysis

The approximate analysis presented above provides insight regarding the mechanism by which and the extent to which the various capacitances limit the high-frequency gain of t he CS (and CE) amplifiers. A node equation at the drain provides

$$sC_{gd}(V_{gs} - V_o) = g_m V_{gs} + \frac{V_o}{R_L'} + sC_L V_o$$

which can be manipulated to the form

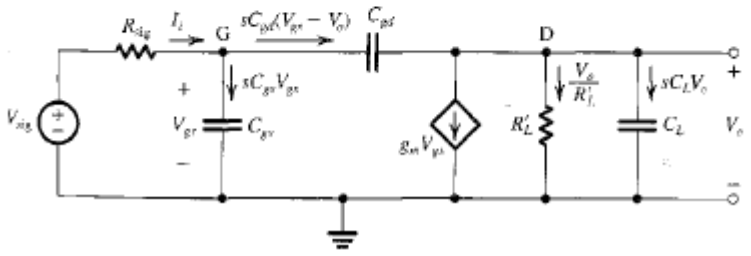
$$V_{gs} = \frac{-V_o}{g_m R_L'} \frac{1 + s(C_L + C_{gd})R_L'}{1 - sC_{gd}/g_m}$$

A loop equation at the input yields

$$V_{sig} = I_i R_{sig} + V_{gs}$$

in which we can substitute for I_i from a node equation at G,

$$I_i = sC_{gs}V_{gs} + sC_{gd}(V_{gs} - V_o)$$



to obtain

$$V_{sig} = V_{gs}[1 + s(C_{gs} + C_{gd})R_{sig}] - sC_{gd}R_{sig}V_o$$

We can now substitute in this equation for V_{gs} from Eq. (6.59) to obtain an equation in V_o and V_{sig} that can be arranged to yield the amplifier gain as

$$\frac{V_o}{V_{sig}} = \frac{-(g_m R'_L)[1 - s(C_{gd}/g_m)]}{1 + s\{[C_{gs} + C_{gd}(1 + g_m R'_L)]R_{sig} + (C_L + C_{gd})R'_L\} + s^2[(C_L + C_{gd})C_{gs} + C_L C_{gd}]R_{sig}R'_L}$$

The above transfer function indicates that the amplifier has a second-order denominator, and hence two poles. Now, since the numerator is of the first order, it follows that one of the two transmission zeros is at infinite frequency. This is readily verifiable by noting that as *s* approaches ∞, *(V0 /* Vsig) approaches zero. The second zero is at

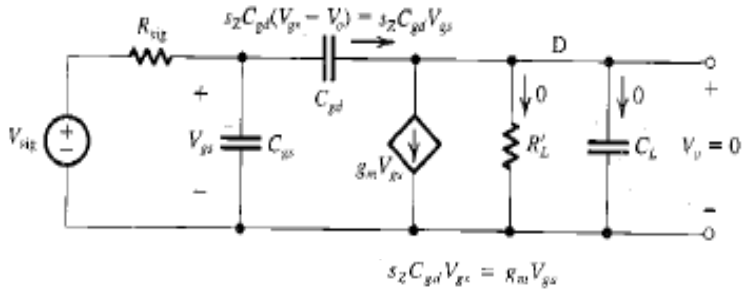
$$s = s_Z = \frac{g_m}{C_{gd}}$$

That is, it is on the positive *real axis* of the s-plane and has a frequency ω_z**,**

$$\omega_Z = g_m / C_{gd}$$

Since ***gm*** is usually large and C_{gd} is usually small, f_z is normally a very high frequency and thus has negligible effect on the value of f_H**.**

It is useful at this point to show a simple method for finding the value of ***s*** at which ***V o*** = 0—that is, ***sz.*** Below Figure shows the circuit at ***s = sz.*** By definition, $V_0 = 0$ and a node equation at D yields



$$s_Z C_{gd} V_{gs} = g_m V_{gs}$$

Now, since V_{gs} is *not* zero (why not?), we can divide both sides by V_{gs} to obtain

$$s_Z = \frac{g_m}{C_{gd}}$$

Before considering the poles, we should note that as ***s*** goes toward zero, K/Vsig approaches the dc gain ***(-g_mR'$_L$),*** as should be the case. Let's now take a closer look at the denominator polynomial. First, we observe that the coefficient of the ***s*** term is equal to the effective time-constant τ_H obtained using the open-circuit time-constants method. Again, this should have been expected since it is the basis for the open-circuit time-constants method. Next, denoting the frequencies of the two poles ω_{p1} and ω_{p2}**,** we can express the denominator polynomial ***D(s)*** as

$$D(s) = \left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)$$
$$= 1 + s\left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right) + \frac{s^2}{\omega_{p1}\omega_{p2}}$$

Now, if $\omega_{p1} >> \omega_{p2}$—that is, the pole at ω_{p1} is dominant—we can approximate ***D(s)*** as

$$D(s) \cong 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}}$$

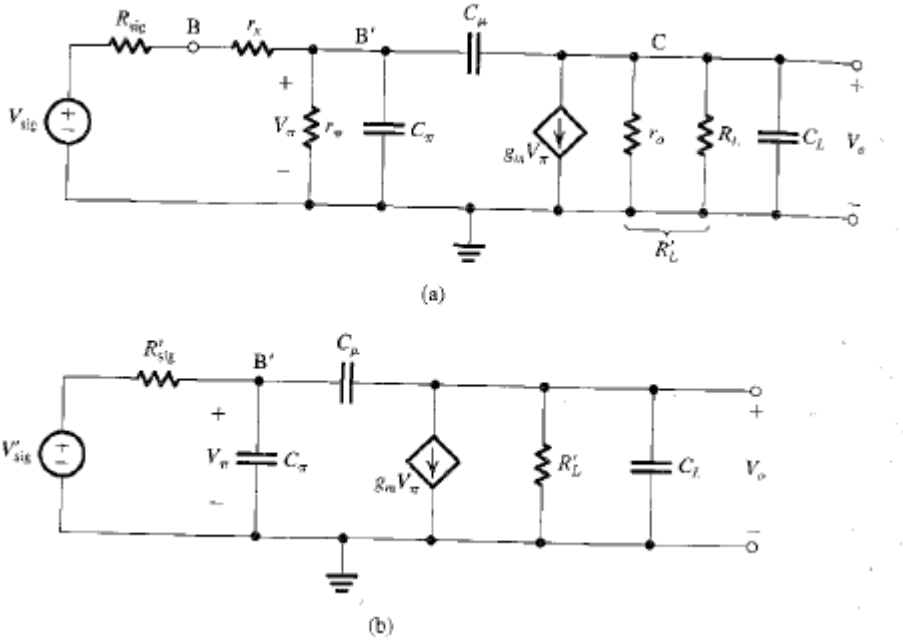
Equating the coefficients of the s term in denominator polynomial

$$\omega_{P1} \cong \frac{1}{[C_{gs} + C_{gd}(1 + g_m R'_L)]R_{sig} + (C_L + C_{gd})R'_L}$$

$$\omega_{P2} = \frac{[C_{gs} + C_{gd}(1 + g_m R'_L)]R_{sig} + (C_L + C_{gd})R'_L}{[(C_L + C_{gd})C_{gs} + C_L C_{gd}]R'_L R_{sig}}$$

2.3.4 Adapting the Formulas for the Case of the CE Amplifier

Adapting the formulas presented above to the case of the CE amplifier is straightforward. First, note from how Vsig and Rsigs are modified to take into account the effect of r_x and r_Π



$$V'_{sig} = V_{sig}\frac{r_\pi}{R_{sig} + r_x + r_\pi}$$

$$R'_{sig} = r_\pi \| (R_{sig} + r_x)$$

Thus the DC gain is now given by

$$A_M = -\frac{r_\pi}{R_{sig} + r_x + r_\pi}(g_m R'_L)$$

Using Millers theorem we obtain

$$C_{in} = C_\pi + C_\mu(1 + g_m R'_L)$$

Correspondingly, the 3-dB frequency f_H can be estimated from

$$f_H \cong \frac{1}{2\pi C_{in} R'_{sig}}$$

Alternatively, using the method of open-circuit time constants yields

$$\begin{aligned}\tau_H &= C_\pi R_\pi + C_\mu R_\mu + C_L C_{C_L} \\ &= C_\pi R'_{sig} + C_\mu[(1 + g_m R'_L)R'_{sig} + R'_L] + C_L R'_L\end{aligned}$$

from which f_H can be estimated as

$$f_H \cong \frac{1}{2\pi\tau_H}$$

The exact analysis yields the following zero frequency:

$$f_Z = \frac{1}{2\pi}\frac{g_m}{C_\mu}$$

and, assuming that a dominant pole exists

$$f_{P1} \cong \frac{1}{2\pi}\frac{1}{[C_\pi + C_\mu(1+g_m R'_L)]R'_{sig} + (C_L + C_\mu)R'_L}$$

$$f_{P2} \cong \frac{1}{2\pi}\frac{[C_\pi + C_\mu(1+g_m R'_L)]R'_{sig} + (C_L + C_\mu)R'_L}{[C_\pi(C_L + C_\mu) + C_L C_\mu]R'_{sig} R'_L}$$

For $f_Z, f_{P2} \gg f_{P1}$,

$$f_H \cong f_{P1}$$

2.3.5 The Situation When R_{sig} Low

There are applications in which the CS amplifier is fed with a low-resistance signal source. Obviously, in such a case, the high-frequency gain will no longer be limited by the interaction
of the source resistance and the input capacitance. Rather, the high-frequency limitation happens at the amplifier output, as we shall now show.
The high-frequency equivalent circuit of the common-source amplifier in the limiting case when R_{sig} is zero. The voltage transfer function V_0 / V sig = *Vo/Vgs* can be found by setting R_{sig} = 0 The result is

$$\frac{V_o}{V_{sig}} = \frac{(-g_m R'_L)[1 - s(C_{gd}/g_m)]}{1 + s(C_L + C_{gd})R'_L}$$

Thus, while the dc gain and the frequency of the zero do not change, the high-frequency response is now determined by a pole formed by *CL + Cgd* together with *R'L*. Thus the 3-dB frequency is now given by

$$f_H = \frac{1}{2\pi(C_L + C_{gd})R'_L}$$

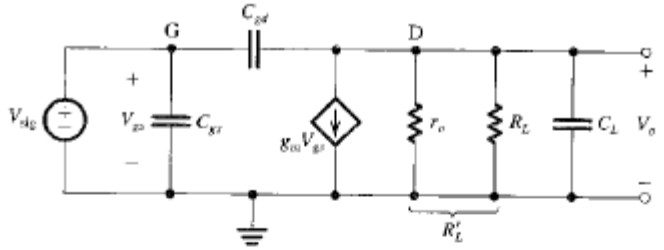
Observe that the circuit reduces to a capacitance *(CL + Cgd)* in parallel with a resistance R'_L.

As we have seen above, the transfer-function zero is usually at a very high frequency and thus does not play a significant role in shaping the high-frequency response. The gain of the CS amplifier will therefore fall off at a rate of - 6 dB/octave (- 20 dB/decade) and reaches unity (0 dB) at a frequency f_t, which is equal to the gain - bandwidth product,

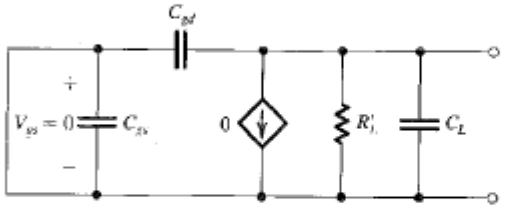
$$f_t = |A_M| f_H$$
$$= g_m R'_L \frac{1}{2\pi(C_L + C_{gd})R'_L}$$

Thus,

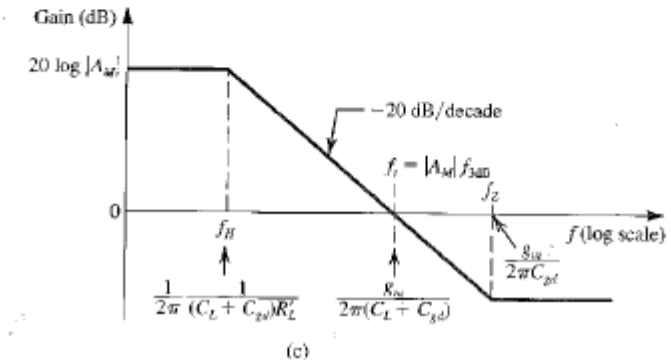
$$f_t = \frac{g_m}{2\pi(C_L + C_{gd})R'_L}$$



(a)



(b)



(c)

2.4 THE CASCODE AMPLIFIER: The Cascode Amplifier, The MOS Cascode, Frequency Response of the MOS Cascode, The BIT Cascode, Darlington configuration

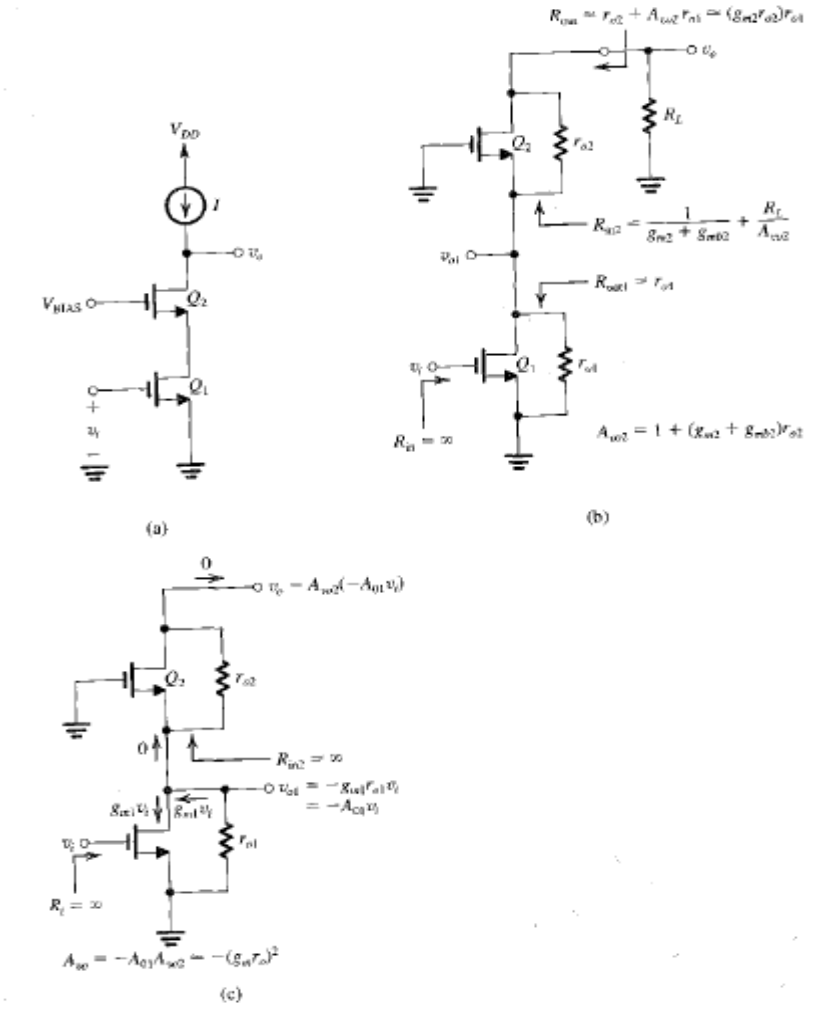
2.4 THE CASCODE AMPLIFIER

By placing a common-gate (common-base) amplifier stage in cascade with a common-source (common-emitter) amplifier stage, a very useful and versatile amplifier circuit results. It is known as the cascode configuration and has been in use for nearly three quarters of a century, obviously in a wide variety of technologies.

The basic idea behind the cascode amplifier is to combine the high input resistance and large trans conductance achieved in a common-source (common-emitter) amplifier with the current-buffering property and the superior high-frequency response of the common-gate (common-base) circuit. As will be seen shortly, the cascode amplifier can be designed to obtain a wider bandwidth but equal dc gain as compared to the common-source (common emitter) amplifier. Alternatively, it can be designed to increase the dc gain while leaving the gain-bandwidth product unchanged. Of course, there is a continuum of possibilities between these two extremes.

Although the cascode amplifier is formed by cascading two amplifier stages, in many applications it is thought of and treated as a single-stage amplifier.

2.4.1 The MOS Cascode



a) The MOS cascode amplifier, (b) The circuit prepared for small-signal analysis with various input and output resistances indicated, (c) The cascode with the output open-circuited.

Above Figure (a) shows the MOS cascode amplifier. Here transistor Q1 is connected in the common-source configuration and provides its output to the input terminal (i.e., source) of transistor Q2 **.** Transistor Q2 has a constant dc voltage, V_{BIAS}, applied to its gate. Thus the signal voltage at the gate of Q2 is zero, and ***Q 2*** is operating as a CG amplifier with a constant current load I . Obviously both Q1 and Q2 will be operating at dc drain currents equal to I.
As in previous cases, feedback in the overall circuit that incorporates the cascode amplifier establishes an appropriate dc voltage at the gate of Q1 so that its drain current is equal to I. Also, the value of V_{BIAS} has to be chosen so that both Q1 and Q2 operate in the saturation region at all times.

Small-Signal Analysis We begin with a qualitative description of the operation of the cascode circuit. In response to the input signal voltage v_i the common-source transistor Q1 conducts a current signal $g_{m1}v_i$ in its drain terminal and feeds it to the source terminal of the common-gate transistor Q2 **,** called the cascode transistor . Transistor Q2 passes the signal current $g_{m1}v_i$ on to its drain, where it is supplied to a load resistance $\boldsymbol{R}_L$ at a very high output resistance, $\boldsymbol{R}$ out **.** The cascode transistor Q2

acts in effect as a buffer, presenting a low input resistance to t he drain of Q1 and providing a high resistance at the amplifier output.

Next we analyze the cascode amplifier circuit to determine its characteristic parameters. Toward that end Fig. (b) shows the cascode circuit prepared for small-signal analysis and with a resistance R_L shown at the output. R_L is assumed to include the output resistance of current source I as well as an actual load resistance, if any. The diagram also indicates various input and output resistances obtained using the results of the analysis of the CS and CG amplifiers in previous sections. Note in particular that the CS transistor Q1 provides the cascode amplifier with an infinite input resistance. Also, at the drain of Q1 looking "downward," we see the output resistance of the CS transistor Q1, r_{o1}. Looking "upward," we see the input resistance of the CG transistor Q2 ,

$$R_{in2} = \frac{1}{g_{m2} + g_{mb2}} + \frac{R_L}{A_{vo2}}$$

where

$$A_{vo2} = 1 + (g_{m2} + g_{mb2})r_{o2}$$

Thus the total resistance between the drain of Q_1 and ground is

$$R_{d1} = r_{o1} \| \left[\frac{1}{g_{m2} + g_{mb2}} + \frac{R_L}{A_{vo2}} \right]$$

$$R_{out} = r_{o2} + A_{vo2} r_{o1}$$

$$R_{out} = r_{o2} + [1 + (g_{m2} + g_{mb2})r_{o2}]r_{o1}$$

$$R_{out} \cong (g_{m2} r_{o2}) r_{o1} = A_0 r_{o1}$$

$$v_i = v_{sig}$$

Thus,

$$G_v = A_v$$

Also, note that the amplifier is unilateral; thus,

$$R_o = R_{out}$$

$$\frac{v_{o1}}{v_i} = -g_{m1} r_{o1} = -A_{01}$$

$$v_o = A_{vo2} v_{o1}$$

Thus,

$$A_{vo} = -A_{01} A_{vo2}$$

$$\cong -A_{01} A_{02}$$

which for the usual case of equal intrinsic gains becomes

$$A_{vo} = -A_0^2 = -(g_m r_o)^2$$

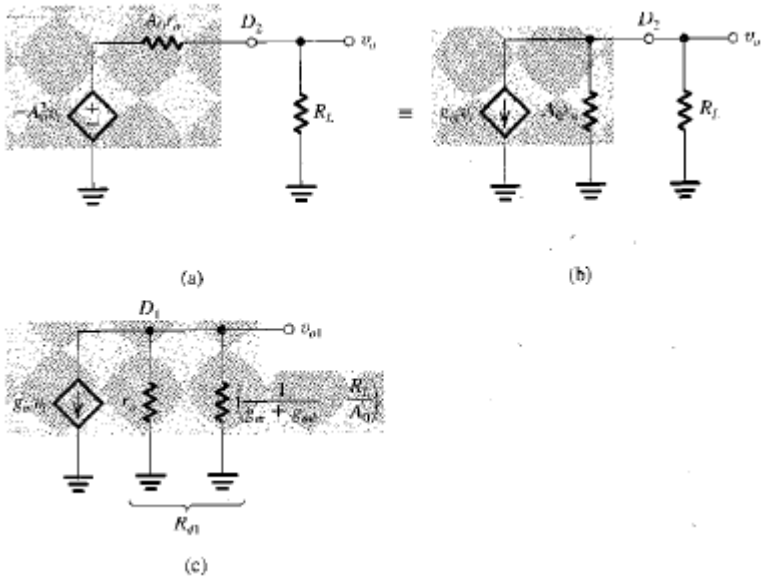
$$A_{vo} = -G_m R_o$$

$$G_m = \frac{A_{01} A_{vo2}}{r_{o2} + A_{vo2} r_{o1}}$$

$$= \frac{g_{m1} r_{o1} [1 + (g_{m2} + g_{mb2}) r_{o2}]}{r_{o2} + [1 + (g_{m2} + g_{mb2}) r_{o2}] r_{o1}}$$

$$\cong g_{m1}$$

The operation of the cascode amplifier should now be apparent: In response to V_i the CS transistor provides a drain current gm_1V_i, which the CG transistor passes on to R_L and, in the process, increases the output resistance by A_0. It is the increase in Rout to A_0r_o that increases the open-circuit voltage gain to $(gm)(A_0ro) = A_0^2$



From the above circuits

$$A_v = -A_0^2 \frac{R_L}{R_L + A_0 r_o}$$

$$R_L = A_0 r_o, \; A_v = -A_0^2/2.$$

$$\frac{v_{o1}}{v_i} = -g_m\left[r_o \| \left(\frac{1}{g_m} + \frac{R_L}{A_0}\right)\right]$$

For $R_L = A_0 r_o$,

$$\frac{v_{o1}}{v_i} = -g_m\left[r_o \| \left(\frac{1}{g_m} + r_o\right)\right]$$

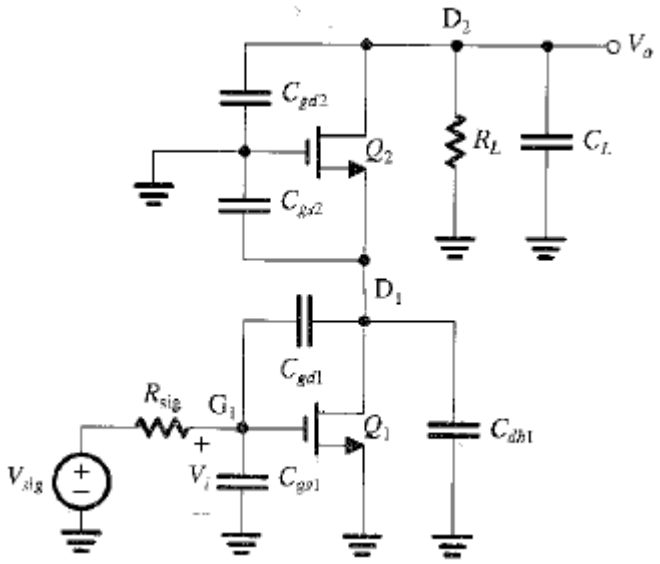
$$\cong -\frac{1}{2} g_m r_o = -\frac{1}{2} A_0$$

$$\frac{v_{o1}}{v_i} = -g_m\left[r_o \| \left(\frac{1}{g_m} + \frac{1}{g_m}\right)\right]$$

$$\cong -2 \text{ V/V}$$

$$A_v = -A_0^2 \frac{r_o}{r_o + A_0 r_o} \cong -A_0$$

2.4.2 Frequency Response of the **MOS** Cascode



Above Figure shows the cascode amplifier with all transistor internal capacitances indicated. Also included is a capacitance C_L at the output node to represent the combination of C_{db2}, the input capacitance of a succeeding amplifier stage (if any), and a load capacitance (if any). Note that C_{dbl} and C_{gs2} appear in parallel, and we shall combine them in the following analysis. Similarly, C_L and C_{gd2} appear in parallel and will be combined.

1. Capacitance C_{gs1} sees a resistance R_{sig}.
2. Capacitance C_{gdl} sees a resistance R_{gdl}, which can be obtained by adapting the formula

$$R_{gd1} = (1 + g_{m1}R_{d1})R_{sig} + R_{d1}$$

3. Capacitance $(C_{dbl} + C_{gs2})$ sees a resistance R_{dl}.
4. Capacitance $(C_L + R_{gd2})$ sees a resistance $(R_L \,\|\, R_{out})$.

With the resistances determined, the effective time constant τ_H can be computed as

$$\tau_H = C_{gs1}R_{sig} + C_{gd1}[(1 + g_{m1}R_{d1})R_{sig} + R_{d1}] + (C_{db1} + C_{gs2})R_{d1} + (C_L + C_{gd2})(R_L \,\|\, R_{out})$$

and the 3-dB frequency f_H as

$$f_H \cong \frac{1}{2\pi\tau_H}$$

To gain insight regarding what limits the high-frequency gain of the MOS cascode amplifier, we rewrite above equation in the form

$$\tau_H = R_{sig}[C_{gs1} + C_{gd1}(1 + g_{m1}R_{d1})] + R_{d1}(C_{gd1} + C_{db1} + C_{gs2}) + (R_L \,\|\, R_{out})(C_L + C_{gd2})$$

In the case of a large Rsig , the first term can dominate, especially if the Miller multiplier $(1 + g_{m1}R_{d1})$ is large. This in turn happens when the load resistance R_L is large (on the order of $A_0 r_o$) , causing Rin2 to be large and requiring the first stage, Q1 to provide a large proportion of the gain. It follows that when jRs i g is large, to extend the bandwidth we have to lower RL to the order of $r0$. This in turn lowers $Rm2$ and hence Rdi and renders the Miller effect insignificant. Note, however, that the dc gain of the cascode will then be A 0 . Thus, while the

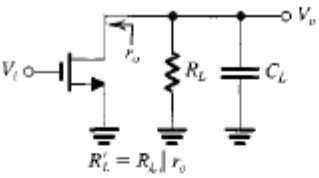
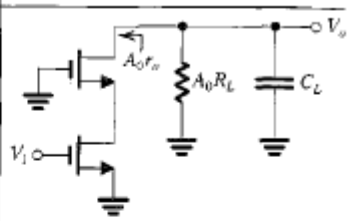
dc gain will b e the same as (or a little higher than) that achieved in a CS amplifier, the bandwidth will be greater.

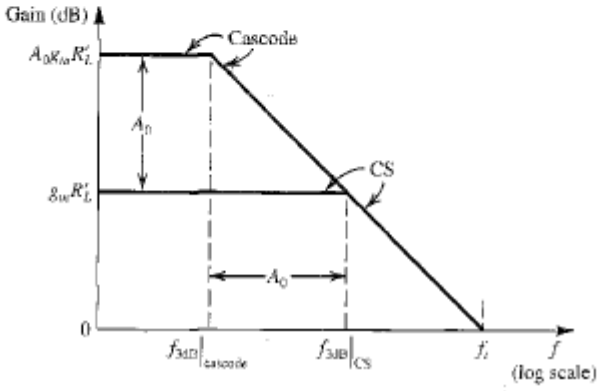
$$\tau_H \cong (C_L + C_{gd2})(R_L \parallel R_{out})$$

and the 3-dB frequency becomes

$$f_H = \frac{1}{2\pi(C_L + C_{gd2})(R_L \parallel R_{out})}$$

$$f_t \cong \frac{1}{2\pi}\frac{g_m}{C_L + C_{gd2}}$$

	Common Source	Cascode
Circuit		
DC Gain	$-g_m R_L'$	$-A_0 g_m R_L'$
f_{3dB}	$\frac{1}{2\pi(C_L + C_{gd})R_L'}$	$\frac{1}{2\pi(C_L + C_{gd})A_0 R_L'}$
f_t	$\frac{g_m}{2\pi(C_L + C_{gd})}$	$\frac{g_m}{2\pi(C_L + C_{gd})}$



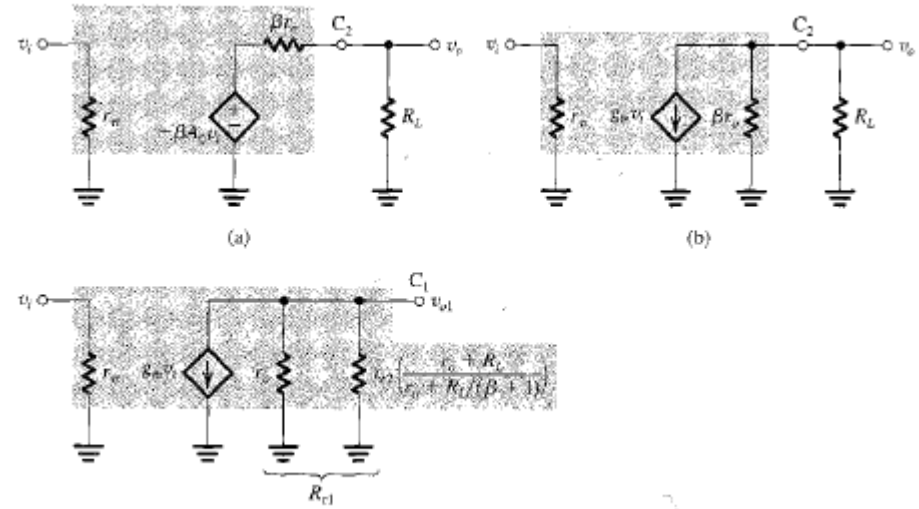
2.4.2 The BJT Cascode

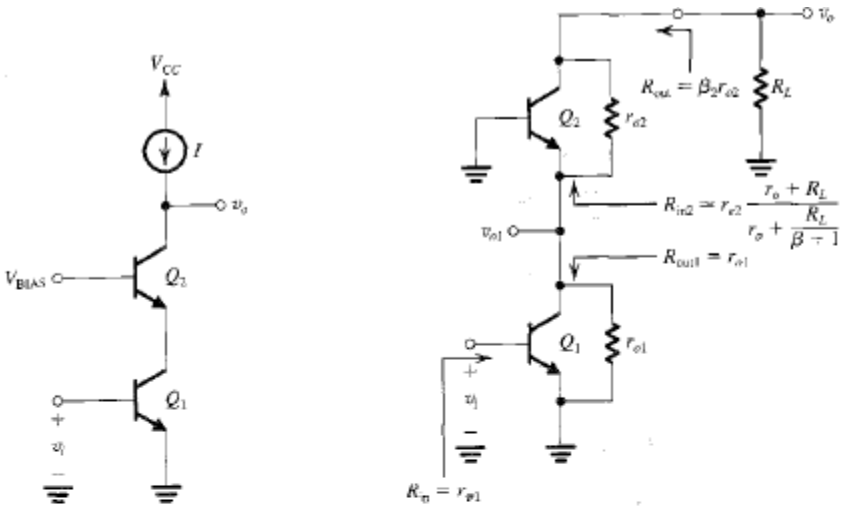
Below Figure shows the BJT cascode amplifier. The circuit is very similar to the MOS cascode, and the small-signal analysis follows in a similar fashion, as indicated in Fig. (b). Here we have shown the various input and output resistances. Observe that unlike the MOSFET cascode, which has an infinite input resistance, the B JT cascode has an input resistance of $r_{\Pi 1}$ (neglecting r_x). The formula for R_{in2} is the one we found in the analysis of the common-base circuit The output resistance Rout= $\beta_2 r_{o2}$ is found by substituting Re = r_{01} and making the approximation that $g_m r_0 >> \beta$. Recall that β r_0 is the largest output resistance that a CB transistor can provide.

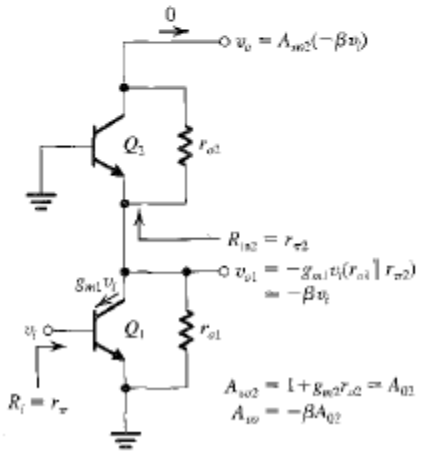
The open-circuit voltage gain *Avo* and the no-load input resistance Ri can be found from the circuit in Fig. (c), in which the output is open-circuited. Observe that Rin2 = $r_{\Pi 2}$, which is

usually much smaller than r_{o1}. As a result the total resistance between the collector of Q1 and ground is approximately $r_{\Pi 2}$; thus the voltage gain realized in the CE transistor Q1 is $-g_{m1} r_{\Pi 2} = -\beta$ • Recalling that the open-circuit voltage gain of a CB amplifier is $(1 + g_m r_0) = A0$, we see that the voltage gain A_{v0} is

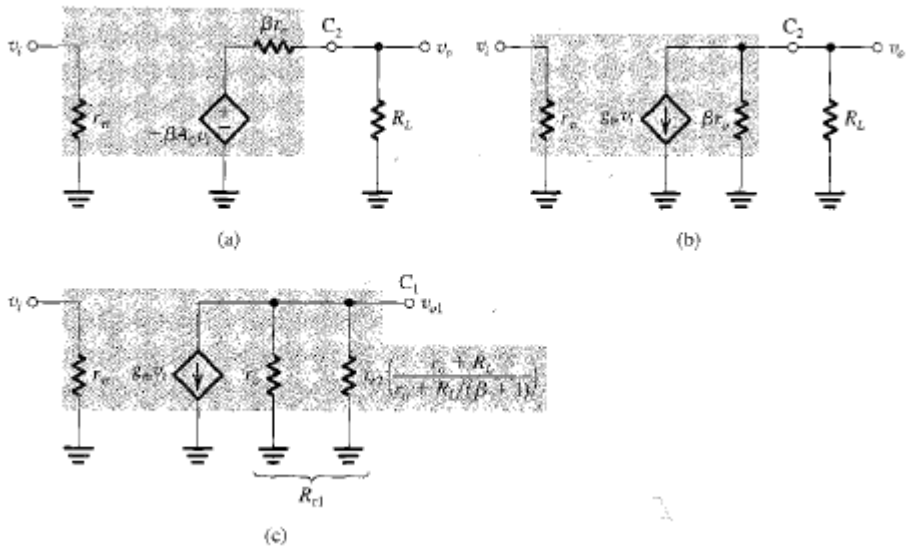
$$A_{v0} = -\beta A_0$$







Putting all of these results together we obtain for the BJT cascode amplifier the equivalent circuit shown in below Fig (a)



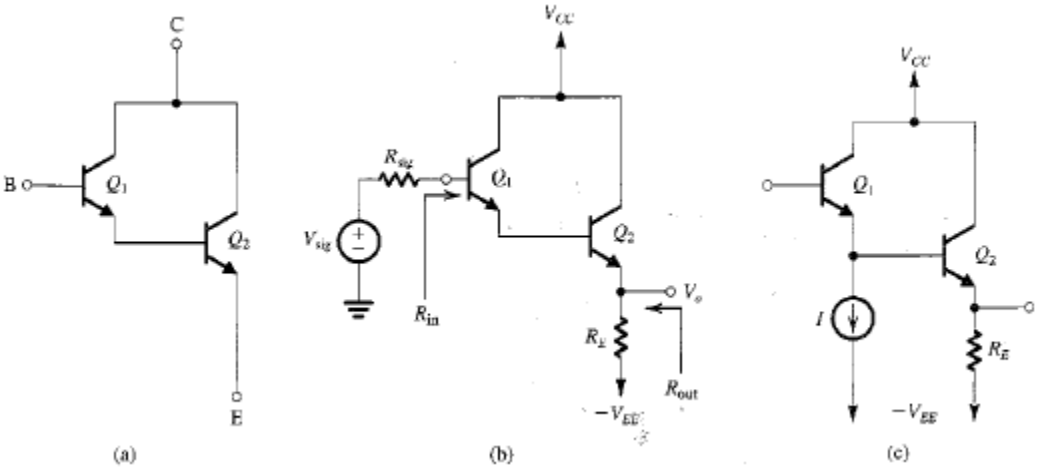
We note that compared to the common-emitter amplifier, cascoding increases both the open circuit voltage gain and the output resistance by a factor equal to the transistor β. This should be contrasted with the factor A_0 encountered in the MOS cascode.

The equivalent circuit can be easily converted to the transconductance form shown in Fig. (b). It shows that the short-circuit transconductance *gm* of the cascode amplifier is equal to the transconductance *gm* of the BJTs. This should have been expected since Q1 provides a current $g_{m1}v_i$ to the emitter of the cascode transistor *Q2,* which in turn passes the current on (assuming $a_2 = 1$) to its collector and to the load resistance R_L. In the process the cascode transistor raises the resistance level from r_0 at the collector of Q1 to βr_0 at the collector of *Q2.* This is the by-now-familiar current-buffering action of the common-base transistor.

The voltage gain of the CE transistor *Qx* can be determined from the equivalent circuit in Fig. (c). The resistance between the collector of Q1 and ground is the parallel equivalent of the output resistance of *Q1, r0,* and the input resistance of the CB transistor, *Q2,* namely R_{in2}. Note that for $R_L < r_0$ the latter reduces to *re,* as expected. However, R_{in2} increases as R_L is increased. Of particular interest is the value of R_{in2} obtained for $R_L = B_{r0}$, namely $Rin2 = r_{\Pi/2}$. It follows that for this value of R_L the CE stage has a voltage gain of $-\beta/2$.

2.5 The Darlington Configuration

Below Figure shows a popular BJT circuit known as the Darlington configuration. It can be thought of as a variation of the CC - CE circuit with the collector of Q1 connected to that of Q2. Alternatively, the Darlington pair can be thought of as a composite transistor with $\boldsymbol{\beta=\beta_1\beta_2}$**.** It can therefore be used to implement a high-performance voltage follower, as illustrated in Fig. (b). Note that in this application the circuit can b e considered as the cascade connection of two common-collector transistors (i.e., a CC - C C configuration).


C
B
Q_1
Q_2
E
(a)
V_{CC}
R_{sig}
Q_1
Q_2
V_{sig}
V_o
R_{in}
R_L
R_{out}
$-V_{EE}$
(b)
V_{CC}
Q_1
Q_2
I
R_E
$-V_{EE}$
(c)

UNIT – III

DIFFERENTIAL AMPLIFIERS

Objectives

- To illustrate MOS and BJT differential amplifierswith common – mode input and differential mode inputs.
- To analyze large-signal and small-signal operation of MOS and BJT differential amplifiers.

Syllabus

MOS differential pair – operation with a common-mode input voltage, operation with a differential input voltage, Large –signal operation, small-signal operation of the MOS differential pair, differential gain, common-mode gain and common-mode rejection ratio (CMRR), frequency-response of resistively loaded MOS differential amplifier, The BJT differential pair – Basic operation, large-signal operation, small-signal operation

Pre-requisites

Studentshould have prior knowledge offundamental circuit analysistechniques and basic electronics background of BJT, MOSFET

Outcomes

Student will be able to

- analyze the MOS and BJT differential pair circuits.
- find the differential gain, common-mode gain, and CMRR of a differential amplifier.
- analyze the frequency response of a differential amplifier.

Introduction

- The differential-pair or differential-amplifier configuration is the most widely used buildingblock in analog integrated-circuit design.
- For instance, the input stage of every op amp is a differential amplifier. Also, the BJT differential amplifier is the basis of a very-high-speed logic circuit family.
- There are two reasons why differential amplifiers are so well suited for IC fabrication:

  - ✓ The performance of the differential pair depends critically on the matching between the two sides of the circuit. Integrated-circuit fabrication is capable of providing matched devices whose parameters track over wide ranges of changes in environmental conditions.
  - ✓ Differential amplifiers utilize more components (approaching twice as many) than single-ended circuits. The advantage of integrated-circuit technology is the availability of large numbers of transistors at relatively low cost.

Why the differential amplifiers are preferred over single-ended amplifiers?

Basically, there are two reasons for using differential in preference to single-ended amplifiers.

1. Differential circuits are much less sensitive to noise and interference thansingle-ended circuits.

   Consider two wires carrying a small differentialsignal as the voltage difference between the two wires. Now, assume that there is an interferencesignal that is coupled to the two wires, either capacitively or inductively. As the twowires are physically close together, the interference voltages on the two wires (i.e., betweeneach of the two wires and ground) will be equal. Since, in a differential system, only the differencesignal between the two wires is sensed, it will contain no interference component!
2. For preferring differential amplifiers is that the differential configurationenables us to bias the amplifier and to couple amplifier stages together without the needfor bypass and coupling capacitors such as those utilized in the design of discrete-circuit amplifiers.

   This is another reason why differential circuits are ideallysuited for IC fabrication where large capacitors are impossible to fabricate economically.

3.1 The MOS differential pair

Figure 3.1 shows the basic MOS differential-pair configuration. It consists of two matchedtransistors, Q_1 and Q_2, whose sources are joined- together and biased by a constant-current source I.

- Assume that the current source is ideal and that it has infinite output resistance.
- Although each drain is shown connected to the positive supply through a resistance R_D, in most cases active (current-source) loads are employed.
- Whatever type of load is used, it is essential that the MOSFETs not enter the triode region of operation.

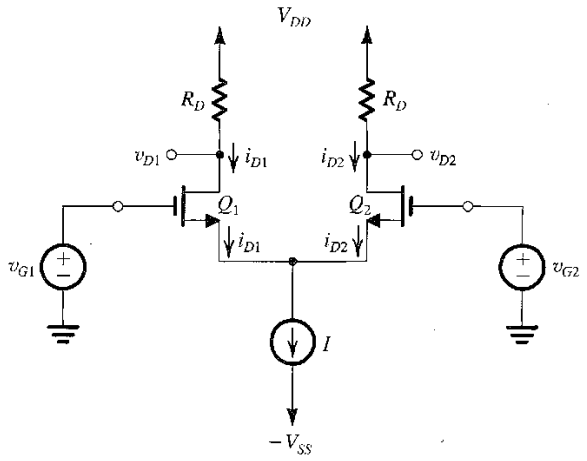


Fig.3.1: The basic MOS differential – pair configuration

3.1.1 Operation with a Common-Mode Input Voltage

- To see how the differential pair works, consider first the case of the two gate terminalsjoined together and connected to a voltage υ_{CM}, called the common-mode voltage.

That is, as shown in Fig. 3.2, $\upsilon_{G1} = \upsilon_{G2} = \upsilon_{CM}$. Since Q_1 and Q_2 are matched, it follows from symmetry that the current / will divide equally between the two transistors. Thus, $i_{D1} = i_{D2} = I/2$, and the voltage at the sources,

$$V_S = V_{CM} - V_{GS} \quad \text{.....(1)}$$

where V_{GS} is the gate-to-source voltage corresponding to a drain current of 1/2. Neglectingchannel-length modulation, V_{GS} and I/2 are related by

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \quad \text{.....(2)}$$

or in terms of the overdrive voltage V_{ov},

$$V_{OV} = V_{GS} - V_t$$

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2$$

$$V_{OV} = \sqrt{I / k_n' (W/L)} \quad \text{.....(3)}$$

The voltage at each drain will be

$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2} R_D \quad \text{.....(4)}$$

Thus, the difference in voltage between the two drains will be zero.

- If the value of the common-mode voltage υ_{CM} is varied, as long as Q_1 and Q_2 remain in the saturation region, the current I will divide equally between Q_1 and Q_2 and the voltages at the drains will not change. Thus the differential pair does not respond to (i.e., it rejects) common-mode input signals.
- An important specification of a differential amplifier is its input common-mode range. This is the range of υ_{CM} over which the differential pair operates properly.

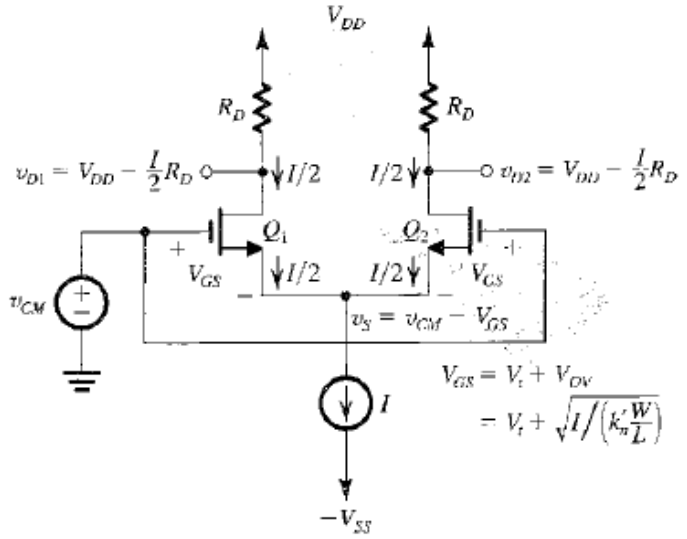


Fig.3.2: The MOS differential pair with a common-mode input voltage, υ_{CM}

- The highest value of υ_{CM} is limited by the requirement that Q_1 and Q_2 remain in saturation,

$$V_{CM\max} = V_t + V_{DD} - \frac{I}{2}R_D \quad \text{.....(5)}$$

- The lowest value of υ_{CM} is determined by the need to allow for a sufficient voltage across current source / for it to operate properly. If a voltage V_{CS} is needed across the current source, then

$$V_{CM\min} = -V_{SS} + V_{CS} + V_t + V_{OV} \quad \text{.....(6)}$$

3.1.2 Operation with a Differential Input Voltage

If we apply a difference or differential input voltage by grounding the gate of Q_2 (i.e.,settingυ_{G2} = 0) and applying a signal υ_{id} to the gate of Q_1 as shown in Fig. 3.3. Since $\upsilon_{id} = \upsilon_{GS1} - \upsilon_{GS2}$.

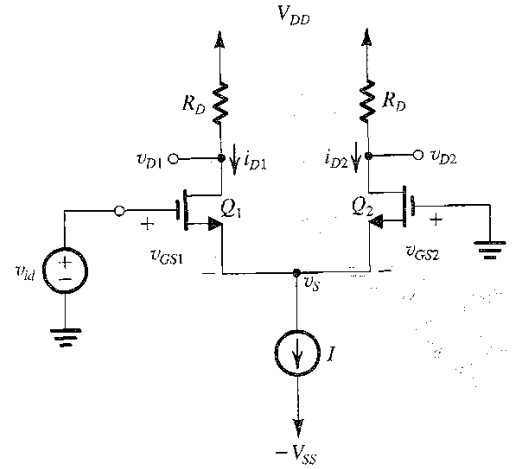


Fig.3.3: The MOS differential pair with a differential input signal υ_{id} applied.

- With υ_{id} positive: $\upsilon_{GS1}>\upsilon_{GS2}$, $i_{D1}>i_{D2}$ and $\upsilon_{D1}<\upsilon_{D2}$, thus ($\upsilon_{D2} - \upsilon_{D1}$) will be positive.
- With υ_{id} negative: $V_{GS1}<\upsilon_{GS2}$, $i_{D1}<i_{D2}$, and $V_{D1}>\upsilon_{D2}$; thus (υ_{D2} - V_{D1}) will be negative.

- From the above, we see that the differential pair responds to difference-mode or differentialinput signals by providing a corresponding differential output signal between the twodrains.
- At this point, it is useful to inquire about the value of υ_{id} that causes the entire biascurrent / to flow in one of the two transistors.
- In the positive direction, this happens when υ_{GS1} reaches the value that corresponds to i_{D1} = I, and υ_{GS2} is reduced to a value equal to thethreshold voltage V_t, at which point υ_S = -V_t. The value of υ_{GS1} can be found from

$$I = \frac{1}{2}\left(k_n' \frac{W}{L}\right)(v_{GS1} - V_t)^2 \quad \text{.....(7)}$$

$$\begin{aligned} v_{GS1} &= V_t + \sqrt{2I/k_n'(W/L)} \\ &= V_t + \sqrt{2}V_{OV} \end{aligned} \quad \text{.....(8)}$$

  whereV_{ov} is the overdrive voltage corresponding to a drain current of I/2.
- Thus, the value of υ_{id} at which the entire bias current I is steered into Q_1 is

$$\begin{aligned} v_{id\max} &= v_{GS1} + v_S \\ &= V_t + \sqrt{2}V_{OV} - V_t \\ &= \sqrt{2}V_{OV} \end{aligned} \quad \text{.....(9)}$$

- If υ_{id} is increased beyond $\sqrt{2}V_{0V}$, i_{D1} remains equal to I, υ_{GS1} remains equal to (V_t + $\sqrt{2}V_{0V}$),and υ_s rises correspondingly, thus keeping Q_2 off.
- In a similar manner we can show that in the negative direction, as υ_{id} reaches -$\sqrt{2}V_{0V}$, Q_1 turns off and Q_2 conducts the entire bias current I.
- Thus the current / can be steered from one transistor to the other by varying υ_{id} in the range

$$-\sqrt{2}V_{OV} \le v_{id} \le \sqrt{2}V_{OV} \quad \text{.....(10)}$$

  which defines the range of differential-mode operation. Finally, observe that we have assumed that Q_1 and Q_2 remain in saturation even when one of them is conducting the entire current I.

3.1.3 Large-Signal Operation

- We derive the expressions for the drain currents i_{D1} and i_{D2} in terms of the input differential signal υ_{id} = υ_{G1} - υ_{G2}.
- Assume that the circuit maintains Q_1 and Q_2 out of the triode region of operation at all times.

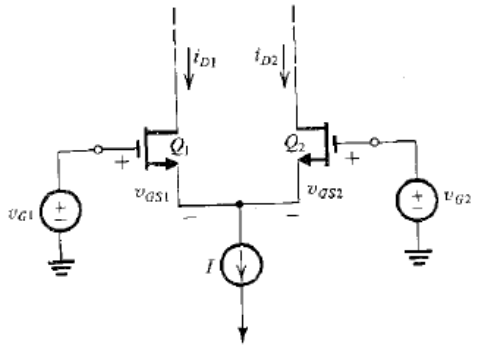


Fig.3.4: The MOSFET differential pair for the purpose of deriving the transfer characteristics, i_{D1} and i_{D2} versus $v_{id} = v_{G1} - v_{G2}$.

- The following derivation assumes that the differential pair is perfectly matched and neglects channel-length modulation (λ = 0) and the body effect.
- To begin with, we express the drain currents of Q_1 and Q_2 as

$$i_{D1} = \frac{1}{2}k_n'\frac{W}{L}(v_{GS1} - V_t)^2 \quad \text{.....(11)}$$

$$i_{D2} = \frac{1}{2}k_n'\frac{W}{L}(v_{GS2} - V_t)^2 \quad \text{.....(12)}$$

Taking the square roots of both sides of each of the above equations, we get

$$\sqrt{i_{D1}} = \sqrt{\frac{1}{2}k_n'\frac{W}{L}}(v_{GS1} - V_t) \quad \text{.....(13)}$$

$$\sqrt{i_{D2}} = \sqrt{\frac{1}{2}k_n'\frac{W}{L}}(v_{GS2} - V_t) \quad \text{.....(14)}$$

Subtracting Eq. 14 from Eq. 13 and substituting

$$v_{GS1} - v_{GS2} = v_{G1} - v_{G2} = v_{id} \quad \text{.....(15)}$$

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2}k_n'\frac{W}{L}}v_{id} \quad \text{.....(16)}$$

The constant-current bias imposes the constraint
Squaring both sides of Eq. 16 and substituting for $i_{D1} + i_{D2} = I$ gives

$$2\sqrt{i_{D1}i_{D2}} = I - \frac{1}{2}k_n'\frac{W}{L}v_{id}^2 \quad \text{.....(17)}$$

Substituting for i_{D2} from Eq. 17 as $i_{D2} = I - i_{D1}$ and squaring both sides of the resulting equation provides a quadratic equation in i_{D1} that can be solved to yield

$$i_{D1} = \frac{I}{2} \pm \sqrt{k_n'\frac{W}{L}I}\left(\frac{v_{id}}{2}\right)\sqrt{1 - \frac{(v_{id}/2)^2}{I/k_n'\frac{W}{L}}} \quad \text{.....(18)}$$

Now, since the increment in i_{D1} above the bias value of I/2 must have the same polarity as v_{id}, only the root with the "+" sign in the second term is physically meaningful; thus,

$$i_{D1} = \frac{I}{2} + \sqrt{k_n'\frac{W}{L}I}\left(\frac{v_{id}}{2}\right)\sqrt{1 - \frac{(v_{id}/2)^2}{I/k_n'\frac{W}{L}}} \quad \text{.....(19)}$$

The corresponding value of i_{D2} is found from $i_{D2} = I - i_{D1}$ as

$$i_{D2} = \frac{I}{2} - \sqrt{k_n' \frac{W}{L} I}\left(\frac{v_{id}}{2}\right)\sqrt{1 - \frac{(v_{id}/2)^2}{I/k_n'\frac{W}{L}}} \quad \text{.....(20)}$$

At the bias (quiescent) point, v_{id}= 0, leading to

$$i_{D1} = i_{D2} = \frac{I}{2} \quad \text{.....(21)}$$

Correspondingly,

$$v_{GS1} = v_{GS2} = V_{GS} \quad \text{.....(22)}$$

Where

$$\frac{I}{2} = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2 = \frac{1}{2}k_n'\frac{W}{L}V_{OV}^2 \quad \text{.....(23)}$$

Now the expressions for i_{D1} and i_{D2} in the alternative form is given as

$$i_{D1} = \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2} \quad \text{.....(24)}$$

$$i_{D2} = \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2} \quad \text{.....(25)}$$

These two equations describe the effect of applying a differential input signal v_{id}on the currents i_{D1} and i_{D2}.

- At v_{id}= 0, the two currents are equal to I/2. Making v_{id} positive causes i_{D1} to increase and i_{D2} to decrease by equal amounts, to keep the sum constant, i_{D1} + i_{D2} = I. The current is steered entirely into $Q1$ when v_{id} reaches the value $\sqrt{2}V_{OV}$.

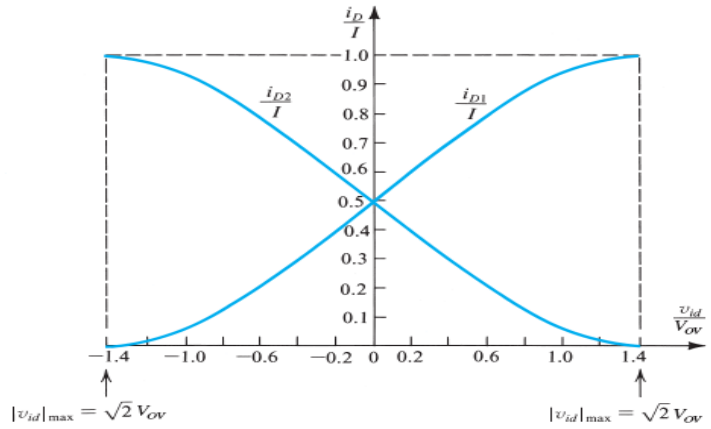


Fig.3.5:Normalized plots of the currents in a MOSFET differential pair. Note that V_{OV} is the overdrive voltage at which Q_1 and Q_2 operate when conducting drain currents equal to I/2, the equilibrium situation. Note that these graphs are universal and apply to any MOS differential pair.

- For v_{id} negative, identical statements can be made by interchanging i_{D1} and i_{D2}. In this case, $v_{id} = -\sqrt{2}V_{OV}$ steers the current entirely into Q_2. Finally, note that the plots in Fig. 3.5 are universal, as they apply to any MOS differential pair.
- The transfer characteristics of Eqs. (24)and(25) and Fig. 3.6 are obviously nonlinear. This is due to the term involving V_{id}^2. Since we are interested in obtaining linear amplification from the differential pair, we will strive to make this term as small as

possible. For a given value of $V_{OV,}$ the only thing we can do is keep $V_{id}/2$ much smaller than V_{OV}, which is the condition for the small-signal approximation. It results in

$$i_{D1} \simeq \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right) \quad \text{.....(26)}$$

And

$$i_{D2} \simeq \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right) \quad \text{.....(27)}$$

which, as expected, indicate that i_{D1} increases by an increment i_d, and i_{D2} decreases by the same amount, i_d, where $i_d$is proportional to the differential input signal v_{id},

$$i_d = \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right) \quad \text{.....(28)}$$

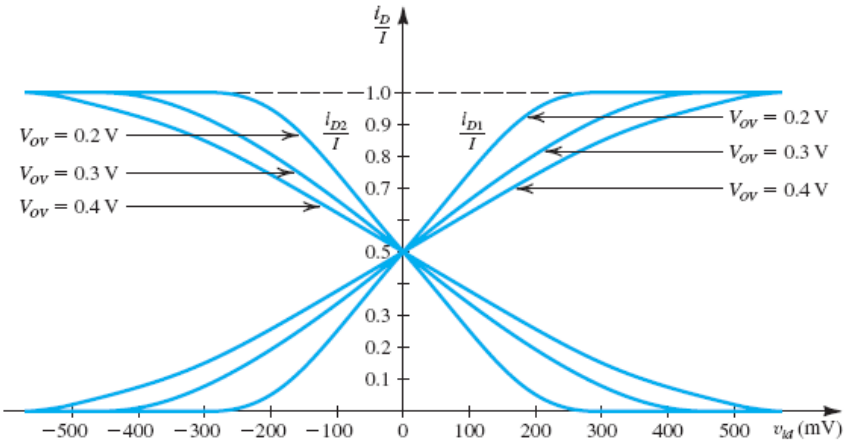


Fig.3.6: The linear range of operation of the MOS differential pair can be extended by operating the transistor at a higher value of V_{OV}.

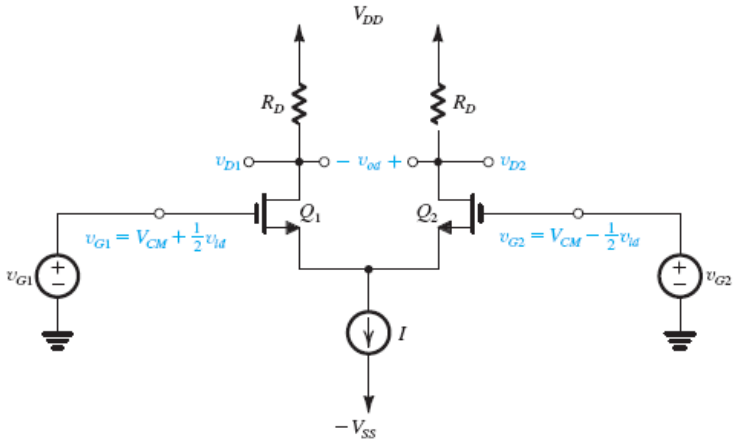
3.2 Small-Signal Operation of the MOS Differential Pair

3.2.1 Differential Gain

Figure 3.7 shows the MOS differential amplifier with input voltages

$$v_{G1} = V_{CM} + \tfrac{1}{2}v_{id} \text{ and}$$

$$v_{G2} = V_{CM} - \tfrac{1}{2}v_{id}$$



(a)

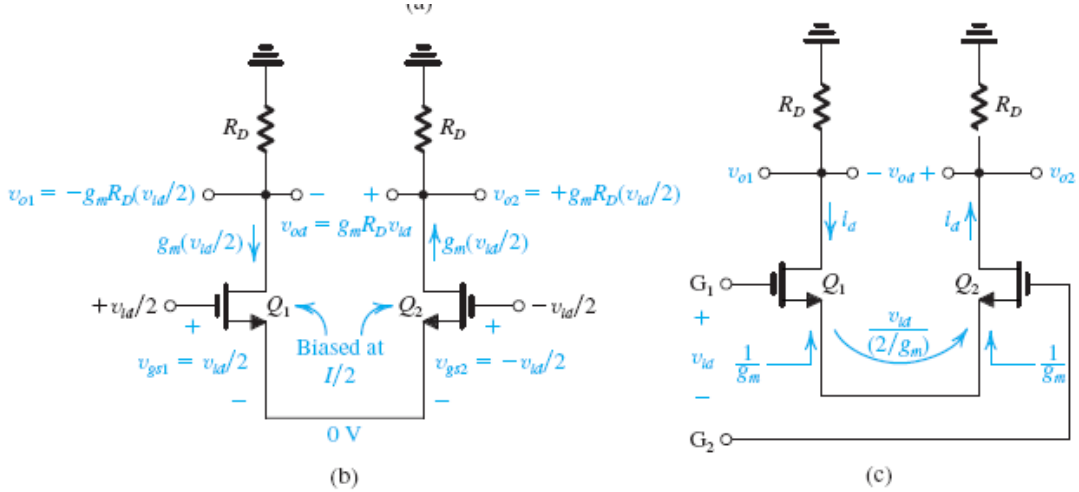


Fig.3.7: Small-signal analysis of the MOS differential amplifier. (a) The circuit with a common-mode voltage applied to set the dc bias voltage at the gates and with v_{id}applied in a complementary (or balanced) manner. (b) The circuit prepared for small-signal analysis. (c) An alternative way of looking at the small signal operation of the circuit.

- Here, V_{CM}denotes a common-mode dc voltage within the input common-mode range of the differential amplifier. It is needed in order to set the dc voltage of the MOSFET gates.Typically$V_{CM}$is at the middle value of the power supply. Thus, for our case, where two complementary supplies are utilized, $V_{CM}$is typically 0V.
- The differential input signal $v_{id}$is applied in a **complementary** (or **balanced**) manner; that is, v_{G1} is increased by $v_{id}/2$and v_{G2} is decreased by $v_{id}/2$.
- If the differential amplifier were fed from the output of another differential-amplifier stage.
- As indicated in above Fig.3.7, the amplifier output can be taken either between one of the drains and ground or between the two drains.
- In the first case, the resulting **single-ended outputs** v_{o1} and v_{o2} will be riding on top of the dc voltages at the drains,V_{DD}-$I/2R_D$.
- This is not the case when the output is taken between the two drains; the resulting **differential** output v_{od}(having a 0-V dc component) will be entirely a signal component.
- To analyze the small-signal operation of the differential amplifier of Fig.3.7(a), and to determine its voltage gain in response to the differential input signal v_{id}.
- From the Fig.3.7 (b), the circuit with the power supplies grounded, the bias current source I removed, and V_{CM}eliminated; that is, only signal quantities are indicated.
- We neglect the effect of the MOSFET r_o. Finally note that each of Q_1 and Q_2 is biased at a dc current of $I/2$ and is operating at an overdrive voltage V_{OV}.
- From the symmetry of the circuit and because of the balanced manner in which $v_{id}$is applied, we observe that the signal voltage at the joint source connection must be zero, acting as a sort of **virtual ground**. Thus Q_1 has a gate-to-source voltage signal $v_{gs1} = V_{id}/2$and Q_2 has $v_{gs2} = -V_{id}/2$.
- Assuming $v_{id}/2 \ll V_{OV}$, the condition for the small-signal approximation, the changes resulting in the drain currents of Q_1 and Q_2 will be proportional to v_{gs1} and v_{gs2}, respectively.
- Thus Q_1 will have a drain current increment $g_m(V_{id}/2)$ and $Q2$ will have a drain current decrement $g_m(V_{id}/2)$,where $g_m$denotes the equal transconductances of the two devices,

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV}} \quad \text{……..(29)}$$

The output voltages for two individual stages are given as

$$v_{o1} = -g_m \frac{v_{id}}{2} R_D \quad \text{…….(30)}$$

$$v_{o2} = +g_m \frac{v_{id}}{2} R_D \quad \text{…….(31)}$$

If the output is taken in a single-ended fashion, the resulting gain becomes

$$\frac{v_{o1}}{v_{id}} = -\frac{1}{2} g_m R_D \quad \text{…….(32)}$$

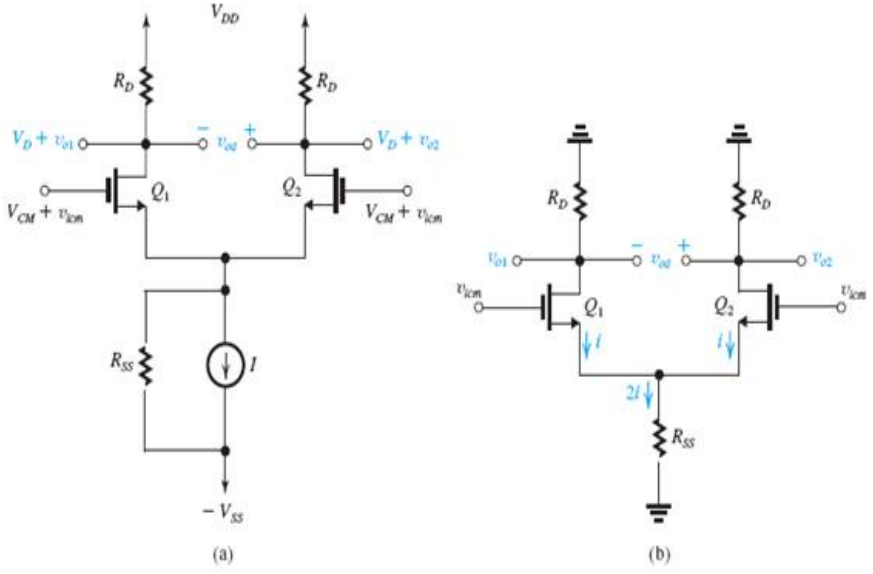
$$\frac{v_{o2}}{v_{id}} = \frac{1}{2} g_m R_D \quad \text{…….(33)}$$

Alternatively, if the output is taken differentially, the gain becomes

$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D \quad \text{…….(34)}$$

3.2.2 Common-Mode Gain and Common-Mode Rejection Ratio (CMRR)

- Figure 3.8 (a) shows a MOS differential amplifier biased with a current source having an output resistance R_{SS}.
- The dc voltage at the input is defined by V_{CM}. Here, however, we also have an incremental signal V_{icm} applied to both input terminals. This common mode input signal can represent an interference signal or noise that is picked up by both inputs and is clearly undesirable.
- To find how much of V_{icm} makes its way to the output of the amplifier, we determine the common-mode gain of the amplifier,analyze the effect of R_{SS} on the bias current of Q_1 and Q_2. That is, with set to zero, the bias current in each of and will no longer be $I/2$ but will be larger than $I/2$ by an amount determined by V_{CM} and R_{SS}.
- However, since R_{SS} is usually very large, this additional dc current in each of Q_1 and Q_2 is usually small and we shall neglect it, thus assuming that and continue to operate at a bias current of $I/2$.



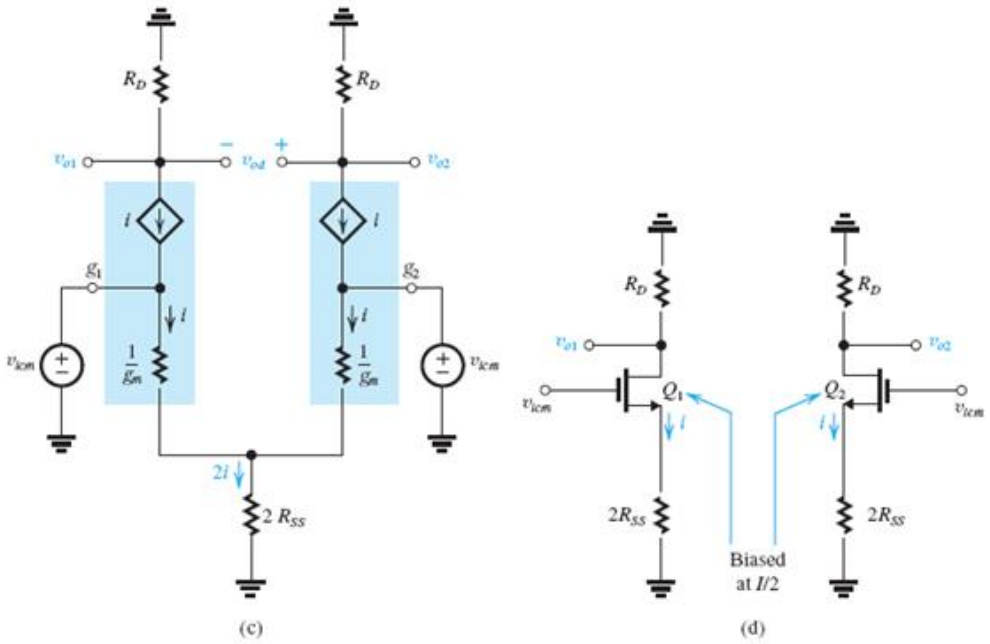


Fig.3.8: (a) A MOS differential amplifier with a common-mode input signal υ_{icm}superimposed on the input dc commonmode voltage V_{CM}. (b) The amplifier circuit prepared for small-signal analysis. (c) The amplifier circuit with the transistors replaced with their T model and $r_o$neglected. (d) The circuit in (b) split into its two halves; each half is called the "CM halfcircuit."

- To determine the response of the differential amplifier to the common-mode input signal, consider the circuit in Fig.3.8, where we have replaced each of V_{DD} and V_{SS} by a short circuit and I by an open circuit.
- The circuit is obviously symmetrical, and thus the two transistors will carry equal signal currents, denoted i. The value of I can be easily determined by replacing each of $Q_1$and Q_2 with its T model and, for simplicity, neglecting r_0. The resulting equivalent circuit is shown in Fig. 3.8(c), from which we can write

$$v_{icm} = \frac{i}{g_m} + 2iR_{SS} \qquad \text{……..……(35)}$$

Thus,

$$i = \frac{v_{icm}}{1/g_m + 2R_{SS}} \qquad \text{……(36)}$$

The voltages at the drain of $Q_1$and Q_2 can now be found as

$$v_{o1} = v_{o2} = -R_D i \qquad \text{……..…(37)}$$

Resulting in

$$v_{o1} = v_{o2} = -\frac{R_D}{1/g_m + 2R_{SS}} v_{icm} \qquad \text{……(38)}$$

Therefore

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \simeq -\frac{R_D}{2R_{SS}} \qquad \text{……..(39)}$$

where we have assumed that $2R_{SS} \gg 1/g_m$ Nevertheless, because $V_{01=}$ V_{02} the differential output voltage V_{0d} will remain free of common-mode interference

$$v_{od} = v_{o2} - v_{o1} = 0 \qquad \text{……(40)}$$

Effect of R_DMismatch

When the two drain resistances exhibit a mismatch ΔR_D as they inevitably do, the common-mode voltages at the two drains will no longer be equal. Rather, if the load of Q_1 is R_D and that of Q_2 is $(R_D + \Delta R_D)$is the drain signal voltages arising from V_{icm} will be

$$v_{o1} \simeq -\frac{R_D}{2R_{SS}} v_{icm} \quad \text{.....(41)}$$

and

$$v_{o2} \simeq -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm} \quad \text{.....(42)}$$

Thus

$$v_{od} = v_{o2} - v_{o1} = -\frac{\Delta R_D}{2R_{SS}} v_{icm} \quad \text{.....(43)}$$

and we can find the common-mode gain A_{CM} as

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = -\frac{\Delta R_D}{2R_{SS}} \quad \text{.....(44)}$$

which can be expressed in the alternate form

$$A_{cm} = -\left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right) \quad \text{.....(45)}$$

- It follows that a mismatch in the drain resistances causes the differential amplifier to have a finite common-mode gain.
- Thus, a portion of the interference or noise signal V_{icm}will appear as a component of V_{od}.
- A measure of the effectiveness of the differential amplifier in amplifying differential-mode signals and rejecting common-mode interference is the ratio of the magnitude of its differential gain(A_d) to the magnitude of its common-mode gain(A_{CM}) This ratio is termed common-mode rejection ratio (CMRR).

Thus,

$$\text{CMRR} \equiv \frac{|A_d|}{|A_{cm}|} \quad \text{.....(46)}$$

and is usually expressed in decibels

$$\text{CMRR (dB)} = 20 \log \frac{|A_d|}{|A_{cm}|} \quad \text{.....(47)}$$

$$\text{CMRR} = \left| (2g_m R_{SS}) \Big/ (\Delta R_D / R_D) \right| \quad \text{.....(48)}$$

Effect of $g_m$mismatch on CMRR

Another possible mismatch between the two halves of the MOS differential pair is a mismatch in g_m of the two transistors. For the purpose of finding the effect of a g_m mismatch on CMRR, let

$$g_{m1} = g_m + \frac{1}{2}\Delta g_m \quad \text{.....(49)}$$

$$g_{m2} = g_m - \frac{1}{2}\Delta g_m \quad \text{.....(50)}$$

That is

$$g_{m1} - g_{m2} = \Delta g_m \quad \text{.....(51)}$$

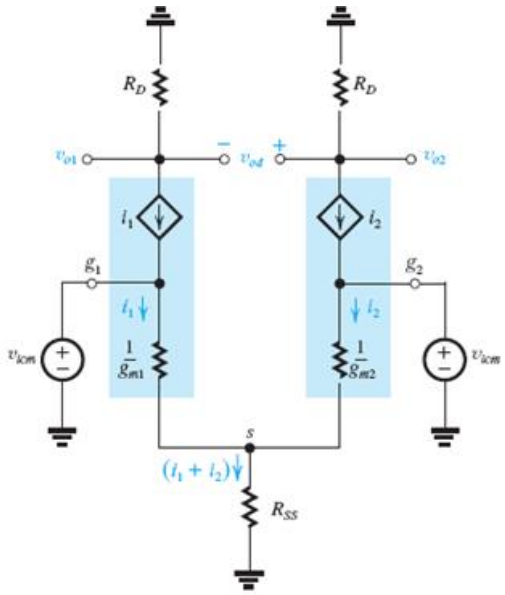


Fig.3.9: Analysis of the MOS differential amplifier with an input common-mode signal v_{icm}in the case the two transistors have a $g_m$mismatch.

Since the circuit is no longer symmetrical, we cannot employ the common-mode half circuit. Rather, we shall return to the original circuit of Fig.3.8 (a) and replace each of $Q_1$and Q_2 and with its T equivalent-circuit model. The result is the equivalent circuit shown in Fig.3.9.

Thus,

$$i_1(1/g_{m1}) = i_2(1/g_{m2}) \quad \text{.....(52)}$$

$$i_1 + i_2 = i_1\left(1 + \frac{g_{m2}}{g_{m1}}\right) \quad \text{.....(53)}$$

3.3 Frequency response of resistively loaded MOS differential amplifier

- The basic resistively loaded MOS differential pair shown in Fig. 3.10(a).It is shown the transistor Q_S that supplies the bias current I. Although we are showing a dc bias voltage V_{BIAS} at its gate, usually Qs is part of a current mirror.
- The total impedance between node S and ground, Z_{SS} plays a significant role in determining the common-mode gain and the CMRR of the differential amplifier.
- Resistance R_{ss} is simply the output resistance of current source Q_s. Capacitance C_{ss} is the total capacitance between node S and ground and includesC_{db} and C_{gd} of Q_s, as well as C_{sb1}, and C_{sb2}. This capacitance can be significant, especially if wide transistors are used for Q_S, Q_1 and Q_2.
- The differential half-circuit shown in Fig. 3.10 (b) can be used to determine the frequency dependence of the differential gain V_0/V_{id}. Indeed the gain function $A_d(s)$ of the differential amplifier will be identical to the transfer function of this common-source amplifier.

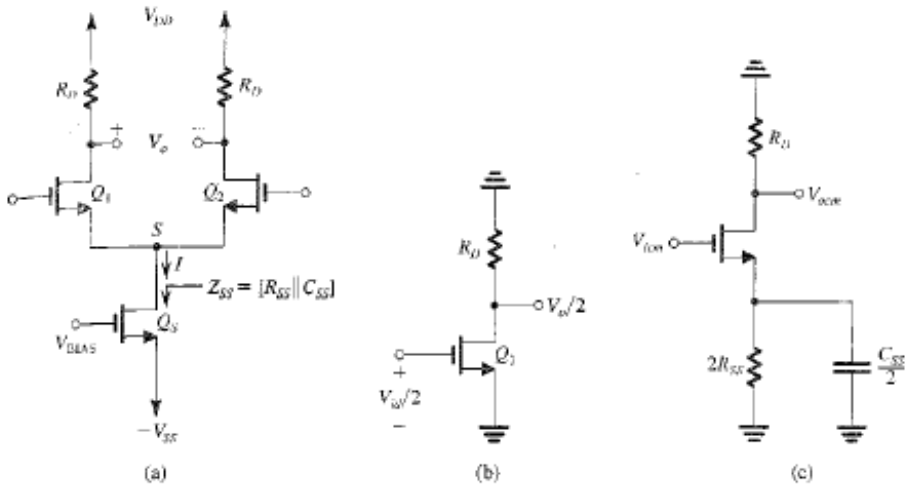


Fig.3.10(a) A resistively loaded MOS differential pair with the transistor supplying the bias currentexplicitly shown. It is assumed that the total impedance between node 5 and ground, Z_{SS}, consists of a resistanceR_{SS}in parallel with a capacitance C_{SS}. (b) Differential half-circuit, (c) Common-mode half-circuit.

- The common-mode half-circuit is shown in Fig.3.10 (c). Although this circuit has other capacitances, namely C_{gs}, C_{gd}, and C_{db} of the transistor in addition to other stray capacitances, we have chosen to show only $C_{SS}/2$. This is because (C_{SS} / 2) together with ($2R_{SS}$) forms a real-axis zero in the common-mode gain function at a frequency much lower than those of the other poles and zeros of the circuit. This zero then dominates the frequency dependence of A_{cm} and CMRR.
- If the output of the differential amplifier is taken single-endedly, then the common-mode gain of interest is V_{ocm}/V_{icm}. More typically, the output is taken differentially.
- Consider what happens when the output is taken differentially andthere is a mismatch ΔR_D between the two drain resistances.

$$A_{cm} = -\left(\frac{R_D}{2R_{SS}}\right)\frac{\Delta R_D}{R_D} \quad \text{.....(54)}$$

which is simply the product of $V_{ocm}/V_{icm}$and the per-unit mismatch $(\Delta R_D / R_D)$.

- Thus, the frequency dependence of A_{cm}can be obtained by simply replacing $R_{SS}$by Z_{SS}in this factor. Doing sofor the expression in Eq. (54) gives

$$\begin{aligned} A_{cm}(s) &= -\frac{R_D}{2Z_{SS}}\left(\frac{\Delta R_D}{R_D}\right) \\ &= -\frac{1}{2}R_D\left(\frac{\Delta R_D}{R_D}\right)Y_{SS} \\ &= -\frac{1}{2}R_D\left(\frac{\Delta R_D}{R_D}\right)\left(\frac{1}{R_{SS}} + sC_{SS}\right) \\ &= -\frac{R_D}{2R_{SS}}\left(\frac{\Delta R_D}{R_D}\right)(1 + sC_{SS}R_{SS}) \end{aligned} \quad \text{.....(55)}$$

from which we see that A_{cm} acquires a zero on the negative real-axis of the s-plane withfrequency ω_Z,

$$\omega_Z = \frac{1}{C_{SS}R_{SS}} \quad \text{.....(56)}$$

$$f_Z = \frac{\omega_Z}{2\pi} = \frac{1}{2\pi C_{SS} R_{SS}} \quad \text{.....(57)}$$

- Usually $f_z$is much lower than the frequencies of the other poles and zeros. As a result, the common-mode gain increases at the rate of +6 dB/octave (20 dB/decade) starting at a relatively low frequency, as indicated in Fig. 3.11(a).
- A_{cm}drops off at high frequencies because of the other poles of the common-mode half-circuit. It is, however, $f_Z$that is significant, for it is the frequency at which the CMRR of the differential amplifier begins to decrease, as indicated in Fig. 3.11(c).

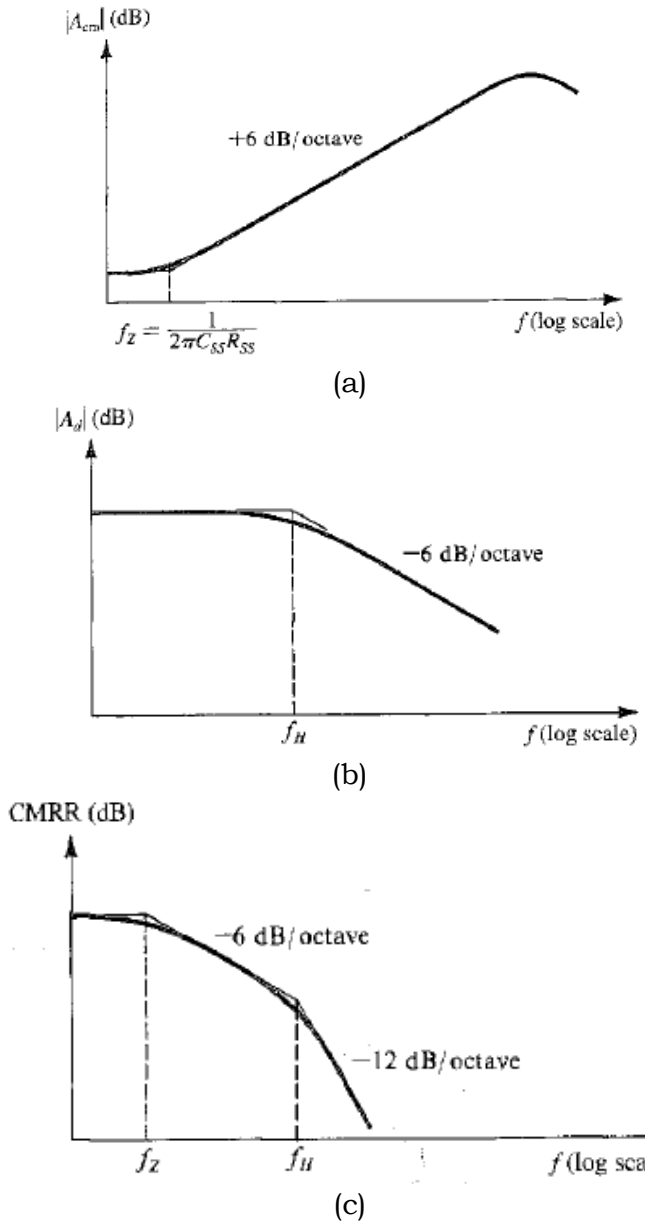


Fig.3.11: Variation of (a) common-mode gain, (b) differential gain, and (c) common-mode rejectionratio with frequency.

- If both $A_d$and $A_{cm}$are expressed and plotted in dB, then CMRR in dB is simply the difference between $A_d$and A_{cm}.
- In order to operate this current source with a small V_{DS} (to conserve the already low V_{DD}), we desire to operate the transistor at a low overdrive voltage Vov.

- For a given value of the current I, however, this means using a large W/L ratio (i.e., a wide transistor). This in turn increases C_{SS} and hence lowers f_Z with the result that the CMRR deteriorates- (i.e., decreases) at a relatively low frequency.
- Thus there is atrade-off between the need to reduce the dc voltage across $Q_S$and the need to keep theCMRR reasonably high at higher frequencies.
- To appreciate the need for high CMRR at higher frequencies, consider the situationillustrated in Fig.3.12

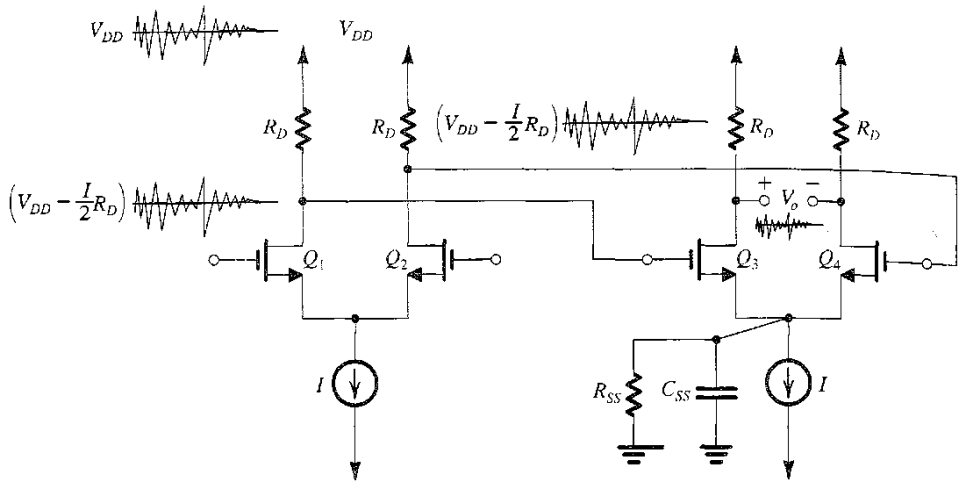


Fig.3.12: The second stage in a differential amplifier is relied on to suppress high-frequency noiseinjected by the power supply of the first stage, and therefore must maintain a high CMRR at higher frequencies.

- We show two stages of a differential amplifier whose power-supplyvoltage $V_{DD}$is corrupted with high-frequency noise.
- Since the quiescent voltage at each of the drains of Q_1 and $Q_2$is $[V_{DD} - (I/2)R_D]$, we see that $\upsilon_{D1}$and υ_{D2}will have the same high frequencynoise as V_{DD}.
- This high-frequency noise then constitutes a common-mode input signal to the second differential stage, formed by $Q_3$and Q_4.
- If the second differential stage is perfectly matched, its differential output voltage V_0should be free of high-frequencynoise.
- In practice there is no such thing as perfect matching and the second stage will have a finite common-mode gain. Because of the zero formed by $R_{SS}$and $C_{SS}$of the second stage, the common-mode gain will increase with frequency, causing some of the noise to make its way to V_0. With careful design, this undesirable component of V_0can be kept small.

3.4 BJT Differential pair

The basic BJT differential-pair configuration is shown in figure 3.13. It is very similar to theMOSFET circuit and consists of two matched transistors, Q_1 and Q_2, whose emitters arejoined together and biased by a constant-current source I.

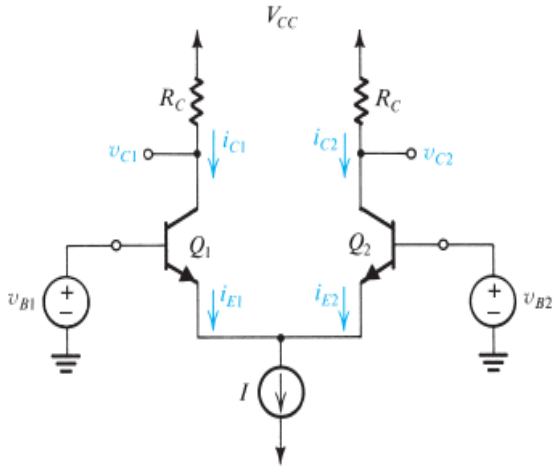


Fig.3.13: The basic BJT differential pair configuration.

3.4.1 Basic Operation

The BJTdifferential-pair also works in two modes Common- mode and differential mode. Consider the case acommon-mode input voltage V_{CM}.

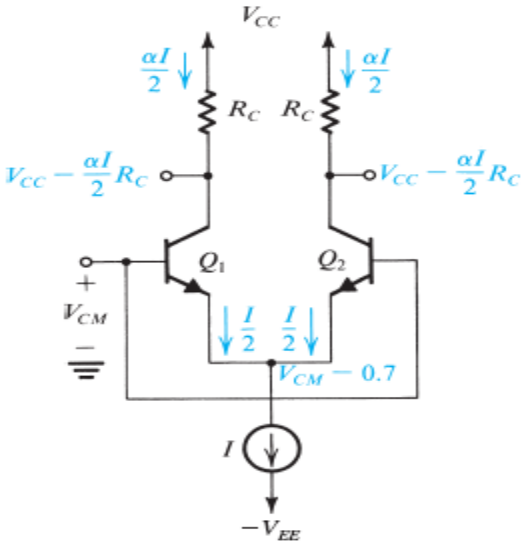


Fig.3.14: (a) The differential pair with a common-mode input voltage V_{CM}

- In this the two bases joined together and connected to a common-mode voltage V_{CM}, i.e$\upsilon_{B1} = \upsilon_{B2} = V_{CM}$.
- Since Q_1 and Q_2 are matched, and assuming an ideal bias current source I with infinite output resistance, it follows that the current I will remain constant and from symmetry that I will divide equally between the two devices.
- Thus $i_{E1} = i_{E2} = I/2$, and the voltage at the emitters will be $V_{CM} - V_{BE}$, where $V_{BE}$is the base–emitter voltage corresponding to an emitter current of I/2 . The voltage at each

collector will be V_{CC}– (1/2) α I R_C, and the difference in voltage between the two collectors will be zero.

- Now let us vary the value of the common-mode input voltage V_{CM}. Obviously, as long as Q_1 and Q_2 remain in the active region and the current source I has sufficient voltage acrossit to operate properly, the current I will still divide equally between Q_1 and Q_2, and the voltages at the collectors will not change.
- Thus the differential pair does not respond to (i.e., it *rejects*) changes in the common-mode input voltage.

3.4.2 The differential pair with a "large" differential input signal

Case (i)

Let the voltage v_{B2} be set to a constant value, say, zero (by grounding B_2), and let v_{B1} = +1 V =>v_{id}>0

- It can be seen that Q_1 will be on and conducting all of the current I and that Q_2 will be off.
- For Q_1 to be on (with V_{BE1} = 0.7 V), the emitter has to be at approximately +0.3 V, which keeps the EBJ of Q_2 reverse-biased.
- The collector voltages will be $v_{C1} = V_{CC}$– α IRC and $v_{C2} = V_{CC}$.

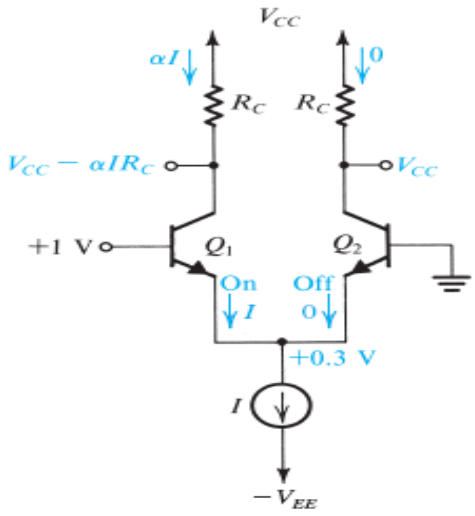


Fig.3.14: (b) the differential pair with a "large" differential input signal; with v_{B1} = +1V and v_{B2} = 0V

- In this case Q_1 conducts entire current, Q_2 is off. Therefore, The collector voltages will be $v_{C1} = V_{CC}$– α $IR_C$and $v_{C2} = V_{CC}$.

Case (ii)

Let the voltage v_{B2} be set to a constant value, say, zero (by grounding B_2), and let v_{B1} = -1 V => v_{id}< 0.

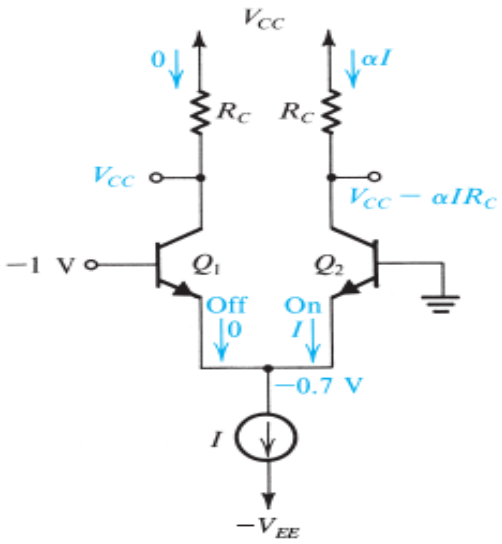


Fig.3.14: (c) the differential pair with a "large" differential input signal; with v_{B1}= -1V and v_{B2} = 0V

- Again with some reasoning it can be seen that Q_1 will turn off, and Q_2 will carry all the current I.
- The common emitter will be at −0.7 V, which means that the EBJ of Q_1 will be reverse biased by 0.3 V. The collector voltages will be $v_{C1} = V_{CC}$and $v_{C2} = V_{CC} - \alpha IR_C$.

3.4.3 The differential pair with a "small" differential input signal

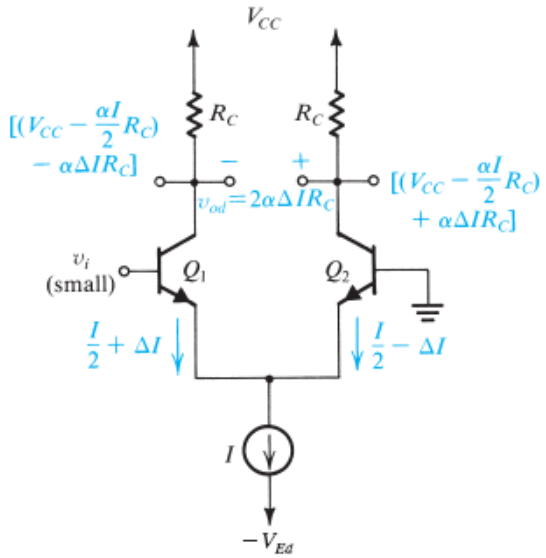


Fig.3.15: The differential pair with a "small" differential input signal applied

- To use the BJT differential pair as a linear amplifier, a very small differential signal (a few millivolts), which will result in one of the transistors conducting a current $\frac{I}{2} + \Delta I$
- The current in the other transistor will be $\frac{I}{2} - \Delta I$, with ΔI being proportional to the difference input voltage. The output voltage taken between the two collectors will be 2α ΔIR_C, which is proportional to the differential input signal v_i.

Input Common-Mode Range

The allowable range of is determined at the upper end by and leaving the active mode and entering saturation.
Thus

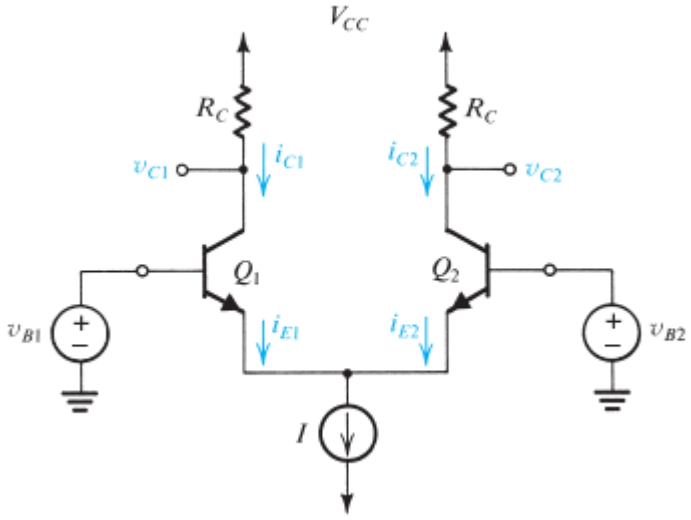
$$V_{CM\max} \simeq V_C + 0.4 = V_{CC} - \alpha\frac{I}{2}R_C + 0.4$$

The lower end of the range is determined by the need to provide a certain minimumvoltage across the current source I to ensure its proper operation. Thus,

$$V_{CM\min} = -V_{EE} + V_{CS} + V_{BE}$$

Large-Signal Operation

Assuming Q_1& Q_2 matched transistors with Bias Emitter current of I/2.



As we know,

$$i_{E1} = \frac{I_S}{\alpha}e^{(v_{B1}-v_E)/V_T}$$

$$i_{E2} = \frac{I_S}{\alpha}e^{(v_{B2}-v_E)/V_T}$$

These two equations can be combined to obtain

$$\frac{i_{E1}}{i_{E2}} = e^{(v_{B1}-v_{B2})/V_T}$$

which can be manipulated to yield

which can be manipulated to yield

$$\frac{i_{E1}}{i_{E1}+i_{E2}} = \frac{1}{1+e^{(v_{B2}-v_{B1})/V_T}}$$

$$\frac{i_{E2}}{i_{E1}+i_{E2}} = \frac{1}{1+e^{(v_{B1}-v_{B2})/V_T}}$$

The circuit imposes the additional constraint

$$i_{E1} + i_{E2} = I$$

Substituting $v_{B1} - v_{B2} = v_{id}$ gives

$$i_{E1} = \frac{I}{1+e^{-v_{id}/V_T}}$$

$$i_{E2} = \frac{I}{1+e^{v_{id}/V_T}}$$

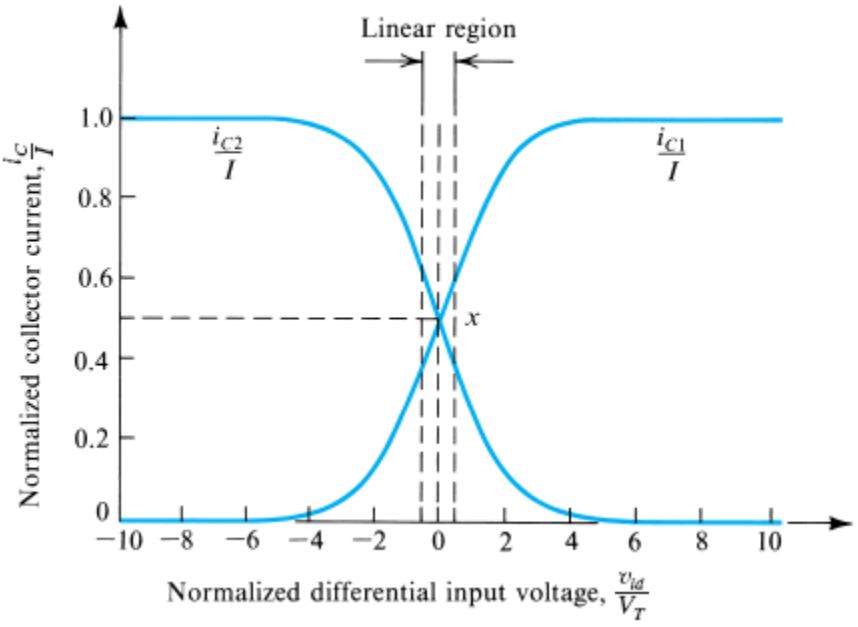


Fig.3.16: Transfer characteristics of the BJT differential pair , assuming $\alpha \cong -1$

Small-Signal Operation

- The BJT differential pair with a difference voltage signal v_{id}applied between the two bases.
- For instance, one of the two input terminals can be grounded and v_{id} applied to the other input terminal. Alternatively, the differential amplifier may be fed from the output of another differential amplifier.

- In thelatter case, the voltage at one of the input terminals will be $VCM + \frac{vid}{2}$ while that at the other input terminal will be $VCM - \frac{vid}{2}$.

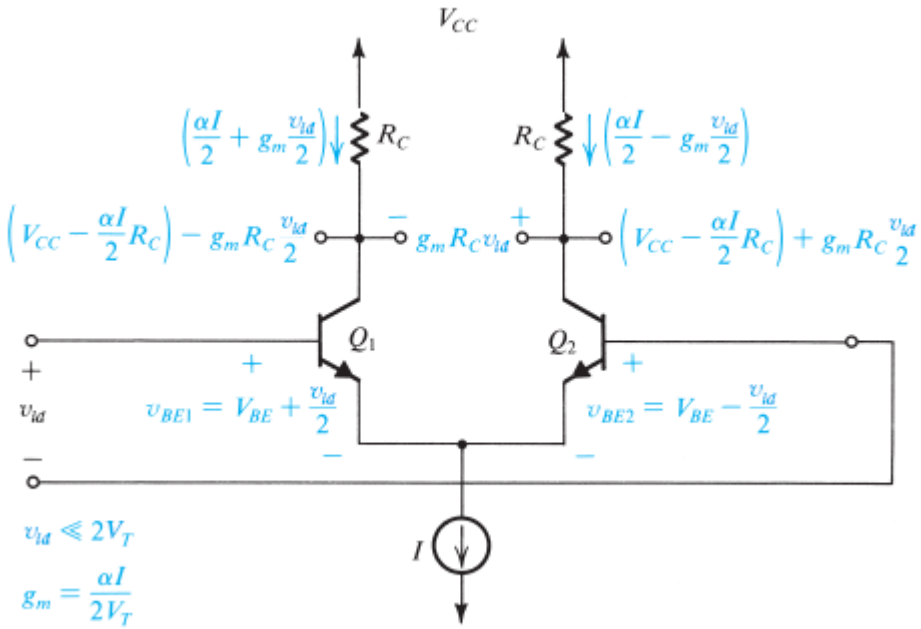


Fig.3.17:The currents and voltages in the differential amplifier when a small differential input signal$v_{id}$is applied.

The collector currents when v_{id}isapplied

$$i_{C1} = \frac{\alpha I}{1 + e^{-v_{id}/V_T}}$$

$$i_{C2} = \frac{\alpha I}{1 + e^{v_{id}/V_T}}$$

Multiplying the numerator and the denominator of the right-hand side

$$i_{C1} = \frac{\alpha I e^{v_{id}/2V_T}}{e^{v_{id}/2V_T} + e^{-v_{id}/2V_T}}$$

Assume that $v_{id} \ll 2V_T$. We may thus expand the exponential in a series and retainonly the first two terms:

$$i_{C1} \simeq \frac{\alpha I(1 + v_{id}/2V_T)}{1 + v_{id}/2V_T + 1 - v_{id}/2V_T}$$

Thus

$$i_{C1} = \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_{id}}{2} \qquad \text{.....(1)}$$

$$i_{C2} = \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_{id}}{2} \qquad \text{.....(2)}$$

- Equations (1) & (2) tell us that when vid = 0, the bias current I divides equally between the two transistors of the pair.
- Thus each transistor is biased at an emitter current of I/2 . When a "small-signal" v_{id} is applied differentially (i.e., between the two bases), the collector current. of Q_1 increases by an increment i_C and that of Q_2 decreases by an equal amount.
- This ensures that the sum of the total currents in Q_1 and Q_2 remains constant, as constrained by the currentsource bias. The incremental (or signal) current component i_C is given by

$$i_c = \frac{\alpha I}{2V_T}\frac{v_{id}}{2}$$

Thus the total base–emitter voltages will be

$$v_{BE}|_{Q1} = V_{BE} + \frac{v_{id}}{2}$$

$$v_{BE}|_{Q2} = V_{BE} - \frac{v_{id}}{2}$$

Where $V_{BE}$is the dc BE voltage corresponding to an emitter current of I/2. Therefore, the collector current of Q_1 will increase by $gm\frac{vid}{2}$and the collector current of Q_2 will decrease by $\frac{vid}{2}$. Here $g_m$denotes the transconductance of Q_1 and of Q_2, which are equal and given by

$$g_m = \frac{I_C}{V_T} = \frac{\alpha I/2}{V_T}$$

Differential Voltage Gain

$$i_{C1} = I_C + g_m\frac{v_{id}}{2}$$

$$i_{C2} = I_C - g_m\frac{v_{id}}{2}$$

Where

$$I_C = \frac{\alpha I}{2}$$

Thus the total voltages at the collectors will be

$$v_{C1} = (V_{CC} - I_C R_C) - g_m R_C\frac{v_{id}}{2}$$

$$v_{C2} = (V_{CC} - I_C R_C) + g_m R_C\frac{v_{id}}{2}$$

- The quantities in parentheses are simply the dc voltages at each of the two collectors.
- As in the MOS case, the output voltage signal of a bipolar differential amplifier can be taken differentially (i.e., between the two collectors, $v_{od} = v_{C2} - v_{C1}$).
- The differential gain of the differential amplifier will be

$$A_d = \frac{v_{od}}{v_{id}} = g_m R_C$$

For the differential amplifier with resistances in the emitter leads,

$$A_d = \frac{\alpha(2R_C)}{2r_e + 2R_e} \simeq \frac{R_C}{r_e + R_e}$$

Common-Mode Gain and CMRR

A bipolar differential amplifier with an input common-mode signal is shown in figure 3.18 (a).

- Here is the output resistance of the bias current source *I*. We wish to find thevoltages that result from at the collectors of Q_1 and Q_2, v_{O1}andv_{O2}between the two collectors.
- Toward that end, we make use of the **common-mode half-circuits.**
- The signal v_{O1}that appears at the collector of in response to will be

$$v_{o1} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm}$$

Similarly v_{O2}, will be

$$v_{o2} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm}$$

where we have neglected the transistor for simplicity. The differential output signalcan be obtained as

$$v_{od} = v_{o2} - v_{o1} = 0$$

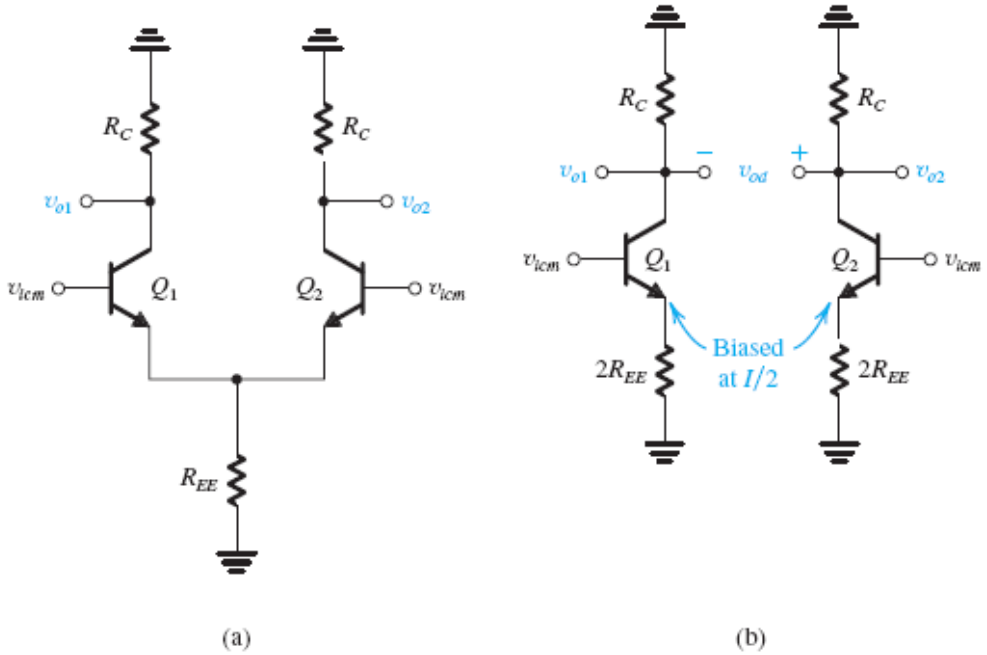


Fig.3.18: (a) The differential amplifier fed by a common-mode input signal v_{icm}. (b)Equivalent"half-circuits" for common-mode calculations.

- Thus, while the voltages at the two collectors will contain common-mode noise or interference components, the output differential voltage will be free from such interference.

- This condition, however, is based on the assumption of perfect matching between the two sides of the differential amplifier. Any mismatch will result inv_{od}acquiring a component proportionaltov$_{icm}$.

Considering R_C Mismatch

Assuming there is a mismatch ΔRc between the two collectorresistances: If the collector of Q_1 has a collector resistanceR_C,

$$v_{o1} = -\frac{\alpha R_C}{2R_{EE} + r_e} v_{icm}$$

and the collector of Q_2 has a collector resistance $(R_C + \Delta R_C)$,

$$v_{o2} = -\frac{\alpha(R_C + \Delta R_C)}{2R_{EE} + r_e} v_{icm}$$

then the differential output voltage v_{od} will be

$$v_{od} \equiv v_{o2} - v_{o1}$$
$$= -\frac{\alpha \Delta R_C}{2R_{EE} + r_e} v_{icm}$$

and the common-mode gain will be

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = -\frac{\alpha \Delta R_C}{2R_{EE} + r_e}$$

$$A_{cm} \simeq -\left(\frac{R_C}{2R_{EE}}\right)\left(\frac{\Delta R_C}{R_C}\right)$$

The common-mode rejection ratio can now be found from

$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|}$$

$$\text{CMRR} = (2g_m R_{EE}) \Big/ \left(\frac{\Delta R_C}{R_C}\right)$$

Input Differential Resistance

- Unlike the MOS differential amplifier, which has an infiniteinput resistance, the bipolar differential pair exhibits a finite input resistance, a result of thefinite β of the BJT.
- The input differential resistance is the resistance seen between the two bases; that is, it is the resistance seen by the differential input signal vid. For the differential amplifier inbelow fig.3.19 (a) &(b) , it can be seen that the base

current of Q_1 shows an increment i_b and the base current of Q_2 shows an equal decrement.

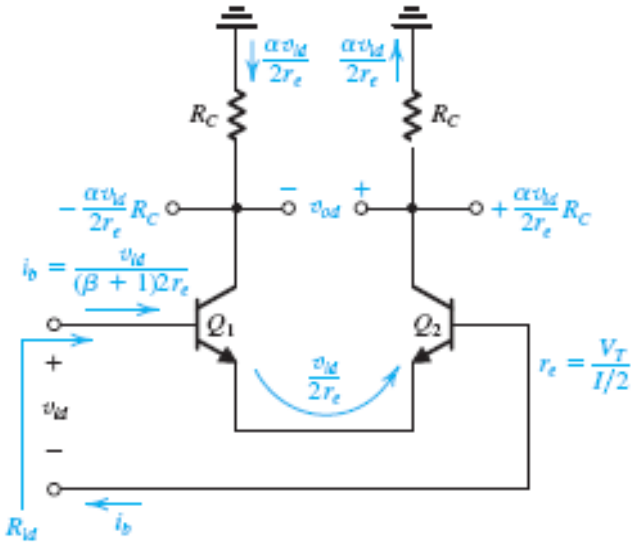


Fig.3.19: (a)A simple technique for determining the signal currents in a differential amplifier excited by adifferential voltage signal v_{id}; dc quantities are not shown.

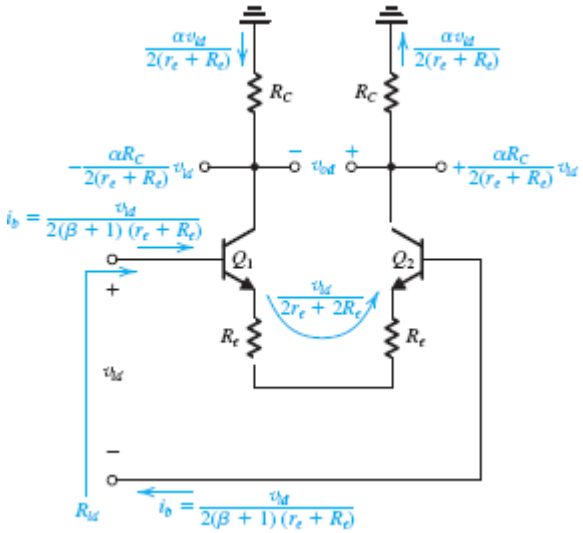


Fig.3.19: (b)A differential amplifier with emitter resistances.

- Thus the collector of Q_1 will exhibit a current increment $i_c$and the collector of Q_2 will exhibit a current decrement i_C:

$$i_c = \alpha i_e = \frac{\alpha v_{id}}{2r_e} = g_m \frac{v_{id}}{2}$$

Each transistor is biased at an emitter current of I/2 .

$$i_e = \frac{v_{id}}{2r_e + 2R_e}$$

$$i_b = \frac{i_e}{\beta + 1} = \frac{v_{id}/2r_e}{\beta + 1}$$

Thus the differential input resistance R_{id} is given by

$$R_{id} \equiv \frac{v_{id}}{i_b} = (\beta + 1)2r_e = 2r_\pi$$

This result is just a restatement of the familiar resistance-reflection rule; namely, *the resistanceseen between the two bases is equal to the total resistance in the emitter circuit multiplied by (*β*+1).*

$$R_{id} = (\beta + 1)(2r_e + 2R_e)$$

UNIT-IV

INTRODUCTION TO OP-AMPS AND TUNED AMPLIFIERS

Objectives:

- To introduce the students about basic block diagram, symbol, specifications and characteristics of an operational amplifier.
- To familiarize with circuit configuration and analysis of tuned amplifiers

SYLLABUS: Ideal op amp, inverting and non-inverting configurations, Tuned amplifiers.

Pre-requisites: Electronic Devices, differential amplifiers

Outcomes:

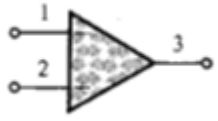
Students will be able to

- Identify the symbol and equivalent notation of an operational amplifier.
- Distinguish between ideal and practical specifications of an operational amplifier.
- Design circuits using operational amplifiers for various linear applications.
- To draw and analyze the behaviour of tuned amplifiers and op amp under inverting and non-inverting configurations.

4.1 THE IDEAL OP AMP

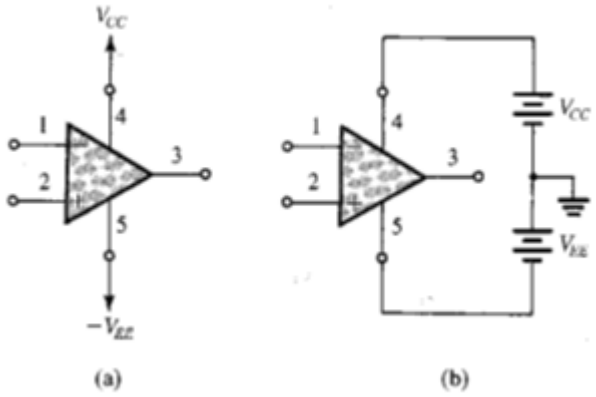
4.1.1 The Op-Amp Terminals

- From a signal point-of-view the op amp has three terminals: two input terminals and one output terminal.
- Below Figure shows the symbol we shall use to represent the op amp. Terminals 1 and 2 are input terminals, and terminal 3 is the output terminal.



Circuit symbol for the op amp

- Below Figure shows two terminals, 4 and 5, are brought out of the op-amp package and connected to a positive voltage Vcc and a negative voltage -VEE, respectively. In Fig. (b).



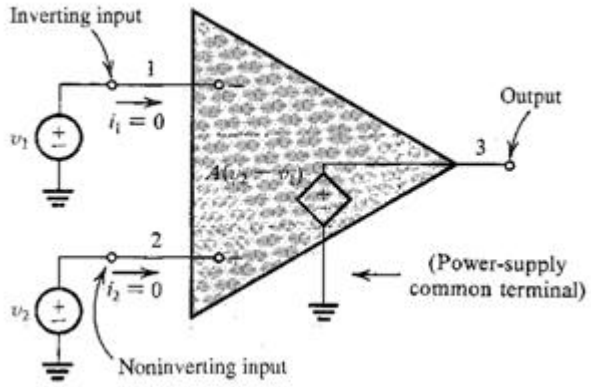
The op amp shown connected to dc power supplies.

- we explicitly show the two dc power supplies as batteries with a common ground. It is interesting to note that the reference grounding point in op-amp circuits is just the common terminal of the two power supplies; that is, no terminal of the op-amp package is physically connected to ground.
- In addition to the three signal terminals and the two power-supply terminals, an op amp may have other terminals for specific purposes. These other terminals can include terminals for frequency compensation and terminals for offset nulling;

4.1.2 Function and Characteristics of the Ideal Op Amp

- We now consider the circuit function of the op amp. The op amp is designed to sense the difference between the voltage signals applied at its two input terminals (i.e., the quantity (v2- v1), multiply this by a number A, and cause the resulting voltage A(v2 – v1) appear at output terminal 3.
- Here it should be emphasized that when we talk about the voltage at a terminal we mean the voltage between that terminal and ground; thus v1 means the voltage applied between terminal 1 and ground.
- The ideal op amp is not supposed to draw any input current; that is, the signal current into terminal 1 and the signal current into terminal 2 are both zero. In other words, the input impedance of an ideal op amp is supposed to be infinite, the output impedance of an ideal op amp is supposed to be zero.
- Putting together all of the above, we arrive at the equivalent circuit model shown in below
- Fig. Note that the output is in phase with (has the same sign as) v2 and is out of phase with (has the opposite sign of) v1. For this reason, input terminal 1 is called the inverting input terminal and is distinguished by a " - " sign, while input terminal 2 is called the non inverting input terminal and is distinguished by a "+" sign.

- As can be seen from the above description, the op amp responds only to the difference signal v2 – v1 and hence ignores any signal common to both inputs. That is, if v1 = v2= 1 V, then the output will—ideally—be zero. We call this property common-mode rejection, and we conclude that an ideal op amp has zero common-mode gain or, equivalently, infinite common-mode rejection.
- For the time being note that the op amp is a differential-input single-ended-output amplifier, with the latter term referring to the fact that the output appears between terminal 3 and ground. Furthermore, gain A is called the differential gain.



- An important characteristic of op amps is that they are direct-coupled or dc amplifiers, where dc stands for direct-coupled. The fact that op amps are direct-coupled devices will allow us to use them in many important applications.
- How about bandwidth? The ideal op amp has a gain A that remains constant down to Zero frequency and up to infinite frequency. That is, ideal op amps will amplify signals of any frequency with equal gain, and are thus said to have infinite bandwidth.
- We have discussed all of the properties of the ideal op amp except for one, which in fact is the most important. This has to do with the value of A. The ideal op amp should have a gain A whose value is very large and ideally infinite.

4.1.3 Differential and Common-Mode Signals

The differential input signal v_{Id} is simply the difference between the two input signals v_1 and v_2; that is, $\boldsymbol{v_{id} = V_2 - V_1}$

The common-mode input signal v_{Icm} is the average of the two input signals *v1* and *v2* namely,

$$v_{Icm} = 1/2\ (v1 + v2)$$

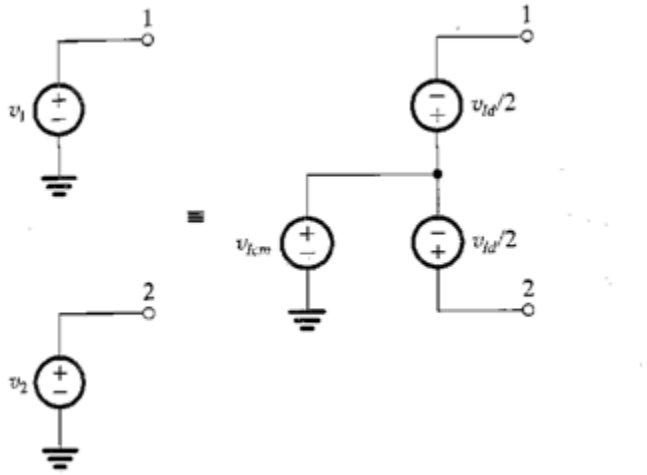
Above equations can b e used to express the input signals v_1 and v_2 in terms of their differential and common-mode components as follows:

$$v_1 = v\ lcm - v\ id / 2$$

and

$$v_2 = vIcm + v\ id / 2$$

These equations can in turn lead to the pictorial representation in below Fig.



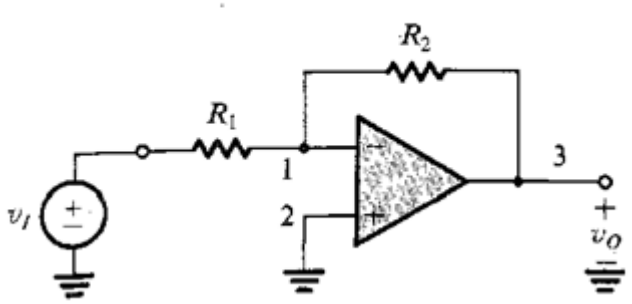
Representation of the signal source v1 and v2 in terms of their differential and common mode components

4.2 THE INVERTING CONFIGURATION

As mentioned above, op amps are not used alone; rather, the op amp is connected to passive components in a feedback circuit. There are two such basic circuit configurations employing an op amp and two resistors: the inverting configuration, which is studied in this section, and the no inverting configuration,

Below Figure shows the inverting configuration. It consists of one op amp and two resistors *R1* and *R2.* Resistor *R2* is connected from the output terminal of the op amp, terminal 3, *back* to the *inverting* or *negative* input terminal, terminal 1. We speak of *R2* as applying **negative feedback;** if *R2* were connected between terminals 3 and 2 we would have called this **positive feedback.**

Note also that *R2 closes the loop* around the op amp. In addition to adding *R2,* we have grounded terminal 2 and connected a resistor *R1* between terminal 1 and an input signal source



The inverting closed loop configuration

with a voltage v_I. The output of the overall circuit is taken at terminal 3 (i.e., between terminal 3 and ground). Terminal 3 is, of course, a convenient point to take the output, since the impedance level there is ideally zero. Thus the voltage *v0* will not depend on the value of the current that might be supplied to a load impedance connected between terminal 3 and ground.

4.2.1 The Closed-Loop Gain

The **closed-loop gain G,** defined as G=Vo/Vi We will do so assuming the op amp to be ideal. Below figure (a) shows the equivalent circuit and the analysis proceeds as follows: The gain A is very large (ideally infinite). If we assume that the circuit is "working" and producing a finite output voltage at

terminal 3, then the voltage between the op amp input terminals should be negligibly small and ideally zero.

Specifically, if we call the output voltage *v0,* then, by definition,

V2-V1= Vo/A= 0

It follows that the voltage at the inverting input terminal *(v_1)* is given by $v_1 = v_2$. That is, because the gain A approaches infinity, the voltage v_1 approaches and ideally equals v_2. We speak of this as the two input tenninals "tracking each other in potential." We also speak of a "virtual short circuit" that exists between the two input terminals. Here the word *virtual* should be emphasized, and one should *not* make the mistake of physically shorting terminals 1 and 2 together while analyzing a circuit. A **virtual short circuit** means that whatever voltage is at 2 will automatically appear at 1 because of the infinite gain A. But terminal 2 happens to be connected to ground; thus $v_2 = 0$ and $v_1 = 0$. We speak of terminal 1 as being a **virtual ground—**

that is, having zero voltage but not physically connected to ground Now that we have determined v_1 we are in a position to apply Ohm's law and find the current i_1 through R_1

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

$$v_O = v_1 - i_1 R_2$$

$$= 0 - \frac{v_I}{R_1} R_2 \qquad \frac{v_O}{v_I} = -\frac{R_2}{R_1}$$

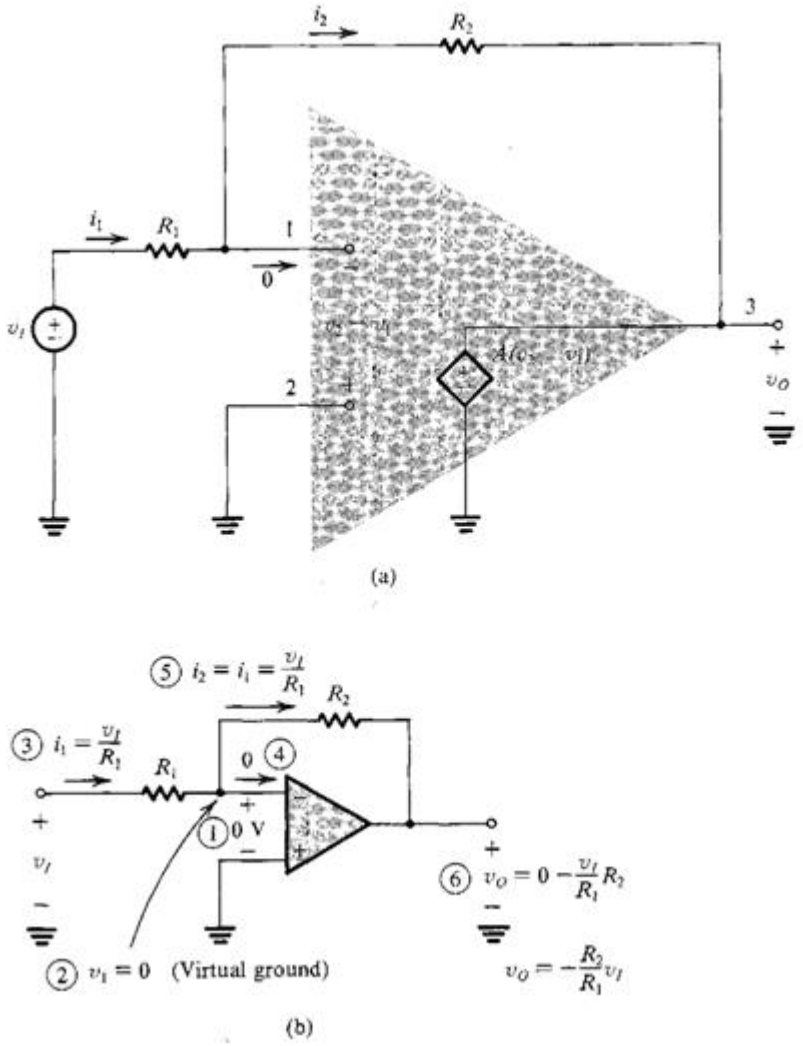


Fig: Analysis of the inverting configuration

Below Figure (b) illustrates these steps and indicates by the circled numbers the order in which the analysis is performed.
We thus see that the closed-loop gain is simply the ratio of the two resistances *R2* and *R1*.
The minus sign means that the closed-loop amplifier provides signal inversion.

The fact that the closed-loop gain depends entirely on external passive components (resistors *R1* and *R2)* is very significant. It means that we can make the closed-loop gain as accurate as we want by selecting passive components of appropriate accuracy. It also means that the closed-loop gain is (ideally) independent of the op-amp gain. This is a dramatic illustration of negative feedback: We started out with an amplifier having very large gain A, and through applying negative feedback we have obtained a closed-loop gain *R2/R1* that is much smaller than *A* but is stable and predictable. That is, we are trading gain for accuracy.

4.2.2 Effect of Finite Open-Loop Gain

The points just made are more clearly illustrated by deriving an expression for the closed loop gain under the assumption that the op-amp open-loop gain A is finite. Below figure shows the analysis. If we denote the output voltage v_0, then the voltage between the two input terminals of the op amp will be v_0/A. Since the positive input terminal is grounded, the voltage at the negative input terminal must be $-v_0/A$. The current *ix* through *Rx* can now be found from

$$i_1 = \frac{v_I - (-v_O/A)}{R_1} = \frac{v_I + v_O/A}{R_1}$$

The infinite input impedance of the op amp forces the current i_1 to flow entirely through *R2*. The output voltage v_0 can thus be determined from

$$v_O = -\frac{v_O}{A} - i_1 R_2$$

$$= -\frac{v_O}{A} - \left(\frac{v_I + v_O/A}{R_1}\right) R_2$$

Collecting terms, the closed-loop gain *G* is found as

$$G \equiv \frac{v_O}{v_I} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

We note that as A approaches infinity, *G* approaches the ideal value of $-R_2/R_1$. Also, from above Fig. we see that as A approaches infinity**,** the voltage at the inverting input terminal approaches zero. This is the virtual-ground assumption we used in our earlier analysis when the op amp was assumed to be ideal.

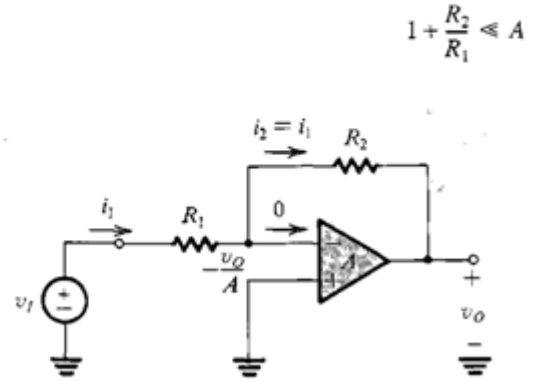


fig:Analysis of the inverting configuation taking into account the infinite open loop gain of the op amp

4.2.3 Input and Output Resistances

Assuming an ideal op amp with infinite open-loop gain, the input resistance of the closed loop inverting amplifier is simply equal to *Rx.* This can be seen

$$R_i \equiv \frac{v_I}{i_1} = \frac{v_I}{v_I/R_1} = R_1$$

we learned that the amplifier input resistance forms a voltage divider with the resistance of the source that feeds the amplifier. Thus, to avoid the loss of signal strength, voltage amplifiers are required to have high input resistance. In the case of the inverting op-amp configuration we are studying, to make *Ri* high we should select a high value for *Rx.* However, if the required gain *R2/R1* is also high, then *R2*

could become impractically large (e.g., greater than a few mega ohms). We may conclude that the inverting configuration suffers from a low input resistance.

4.2.4 An Important Application-The Weighted Summer

A very important application of the inverting configuration is the weighted-summer circuit shown in below Fig. Here we have a resistance R_f in the negative-feedback path (as before), but we have a number of input signals $v_1, v_2, \ldots, v_n$ each applied to a corresponding resistor $R_1, R_2, \ldots, R_n$, which are connected to the inverting terminal of the op amp. From our previous discussion, the ideal op amp will have a virtual ground appearing at its negative input terminal. Ohm's law then tells us that the currents $i_1, i_2, \ldots, i_n$ are given by

$$i_1 = \frac{v_1}{R_1}, \qquad i_2 = \frac{v_2}{R_2}, \qquad \ldots, \qquad i_n = \frac{v_n}{R_n}$$

4.3 THE NONINVERTING CONFIGURATION

The second closed-loop configuration we shall study is shown in below Fig. Here the input signal v_1 is applied directly to the positive input terminal of the op amp while one terminal of R_1 is connected to ground.

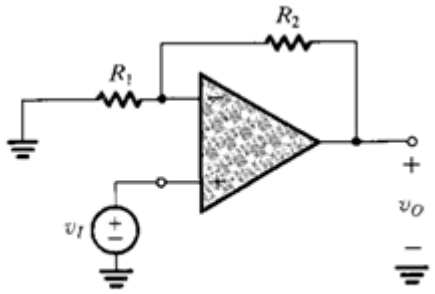


Fig: The non inverting configuration

4.3.1 The Closed-Loop Gain

Analysis of the non inverting circuit to determine its closed-loop gain (v_0/v_1) is illustrated in below Fig. Notice that the order of the steps in the analysis is indicated by circled numbers.

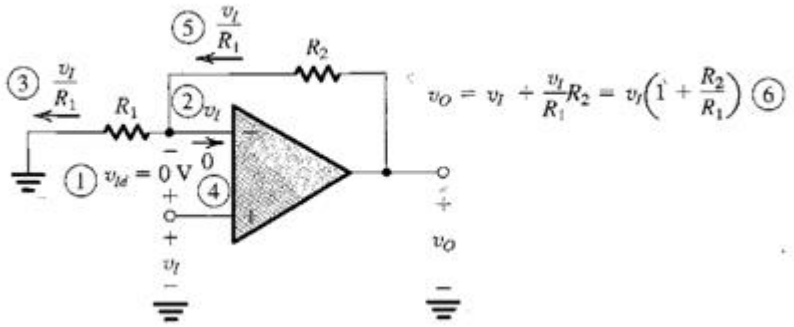


Fig: Analysis of non inverting configuration

Assuming that the op amp is ideal with infinite gain, a virtual short circuit exists between its two input terminals. Hence the difference input signal is

$$v_{Id} = \frac{v_O}{A} = 0 \qquad \text{for } A = \infty$$

Thus the voltage at the inverting input terminal will be equal to that at the non inverting input terminal, which is the applied voltage *vi.* The current through *Ri* can then be determined as *vi/Ri.* Because of the infinite input impedance of the op amp, this current will flow through *R2,* as shown in Fig. Now the output voltage can be determined from

$$v_O = v_I + \left(\frac{v_I}{R_1}\right)R_2$$

$$\frac{v_O}{v_I} = 1 + \frac{R_2}{R_1}$$

Further insight into the operation of the non inverting configuration can be obtained by considering the following: Since the current into the op-amp inverting input is zero, the circuit composed of *R1* and *R2* acts in effect as a voltage divider feeding a fraction of the output voltage back to the inverting input terminal of the op amp; that is,

$$v_1 = v_O\left(\frac{R_1}{R_1 + R_2}\right)$$

Then the infinite op-amp gain and the resulting virtual short circuit between the two input terminals of the op-amp forces this voltage to be equal to that applied at the positive input terminal; thus

$$v_O\left(\frac{R_1}{R_1 + R_2}\right) = v_I$$

4.3.2 Characteristics of the Non inverting Configuration

The gain of the non inverting configuration is positive—hence the name *non inverting.* The input impedance of this closed-loop amplifier is ideally infinite, since no current flows into the positive input terminal of the op amp. The output of the non inverting amplifier is taken at the terminals of the ideal voltage source $A(v_2 - v_1,)$ thus the output resistance of the non inverting configuration is zero.

4.3.3 Effect of Finite Open-Loop Gain

As we have done for the inverting configuration, we now consider the effect of the finite op-amp open-loop gain A on the gain of the non inverting configuration. Assuming the op amp to be ideal except for having a finite open-loop gain A, it can be shown that the closed-loop gain of the non inverting amplifier circuit is given by

$$G \equiv \frac{v_O}{v_I} = \frac{1 + (R_2/R_1)}{1 + \dfrac{1 + (R_2/R_1)}{A}}$$

Observe that the denominator is identical to that for the case of the inverting configuration This is no coincidence; it is a result of the fact that both the inverting and the non inverting configurations have the same feedback loop, which can be readily seen if the input signal source is eliminated (i.e., short-circuited). The numerators, however, are different, for the numerator gives the ideal or nominal closed-loop gain *(-R2/R1* for the inverting configuration, and 1 + *R2/R1* for the non inverting

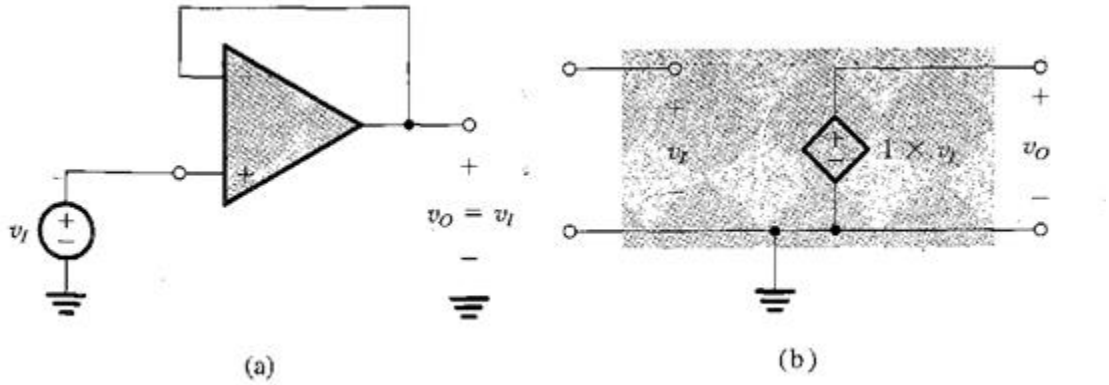
configuration). Finally, we note (with reassurance) that the gain expression reduces to the ideal value for A = infinity. In fact, it approximates the ideal value for

$$A \gg 1 + \frac{R_2}{R_1}$$

This is the same condition as in the inverting configuration, except that here the quantity on the right-hand side is the nominal closed-loop gain.

4.3.4 The Voltage Follower

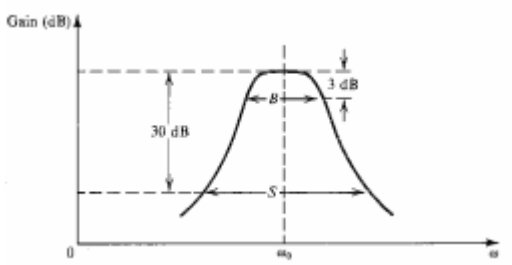
The property of high input impedance is a very desirable feature of the non inverting configuration. It enables using this circuit as a buffer amplifier to connect a source with a high impedance to a low-impedance load. In many applications the buffer amplifier is not required to provide any voltage gain; rather, it is used mainly as an impedance transformer or a power amplifier. In such cases we may make *R2* = 0 and *Rt* = °° to obtain the **unity-gain amplifier** shown in Below Fig.This circuit is commonly referred to as a **voltage follower,** since the output "follows" the input. In the ideal case, *v0 = v1 Rin = ∞, Rout* = 0, and the follower has the equivalent circuit shown in Fig. (b). Since in the voltage-follower circuit the entire output is fed back to the inverting input, the circuit is said to have 100% negative feedback. Since the non inverting configuration has a gain greater than or equal to unity, depending on the choice of *R2/R1*, some prefer to call it "a follower with gain."



The unity gain buffer or follower amplifier and its equivalent circuit model

Tuned Amplifiers:

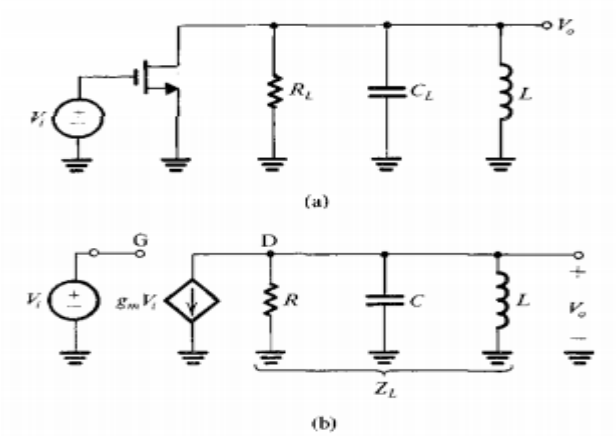
- Tuned Amplifiers are the special kind of frequency selective networks.
- The shape of the frequency response of a tuned amplifier (f_0) is shown in below figure.
- Tuned Amplifiers are mainly used in video and radiofrequency applications and also in radio transmitters and receivers.
- Tuned Amplifiers behaves like narrow band pass filters with very narrow bandwidth.
- Tuned Amplifiers has a very high gain at centre frequency and gain drops at all other frequencies.



Frequency response of a tuned amplifier

Basic Principle:

The basic principle underlying the design of tuned amplifiers is the use of a parallel LCR circuit as the load, or at the input, of a BJT or a FET amplifier. This is illustrated in below figure, with a MOSFE T amplifier having a tuned-circuit load. For simplicity, the bias details are not included. Since this circuit uses a single tuned circuit, it is known as a single-tuned amplifier. The amplifier equivalent circuit is shown . Here R denotes the parallel equivalent of RL and the output resistance r,, of the FET, and C is the parallel equivalent of CL and the FET output capacitance (usually very small). From the equivalent circuit we can write



MOSFET based tuned amplifier and its equivalent circuit

$$V_o = \frac{-g_m V_i}{Y_L} = \frac{-g_m V_i}{sC + 1/R + 1/sL} \quad \textbf{..... (1)}$$

Thus the voltage gain can be expressed as

$$\frac{V_o}{V_i} = -\frac{g_m}{C}\frac{s}{s^2 + s(1/CR) + 1/LC}$$

which is a second-order band pass function. Thus the tuned amplifier has a center frequency of

$\omega_0 = 1/\sqrt{LC}$ and

Band width of

$$B = \frac{1}{CR}$$

And the Quality factor (Q) is given as

$$Q \equiv \omega_0/B = \omega_0 CR$$

Inductor Losses:

The power loss in the inductor is usually represented by a series resistance r_s as shown in Fig. 3(a). However, rather than specifying the value of r_s, the usual practice is to specify the inductor Q factor at the frequency of interest,

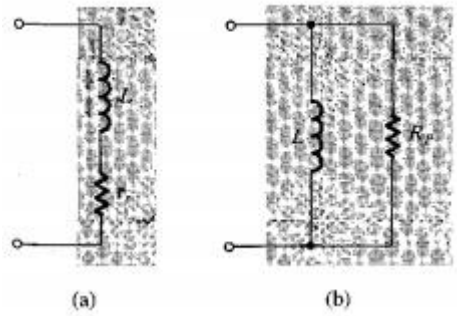
$$Q_0 = \frac{\omega_0 L}{r_s}$$

Typically Q_0 has the value of 50 to 100.

The analysis of a tuned amplifier is greatly simplified by representing the inductor loss by a parallel resistance R_p, as shown . The relationship between R_p and Q_0 can be found b y writing, for the admittance of the circuit in

$$Y(j\omega_0) = \frac{1}{r_s + j\omega_0 L}$$

$$= \frac{1}{j\omega_0 L} \frac{1}{1 - j(1/Q_0)} = \frac{1}{j\omega_0 L} \frac{1 + j(1/Q_0)}{1 + (1/Q_0^2)}$$



(a) series R-L circuit and (b) Parallel R-L circuit

For $Q_0 >> 1$

$$Y(j\omega_0) \simeq \frac{1}{j\omega_0 L}\left(1 + j\frac{1}{Q_0}\right)$$

$$Q_0 = \frac{R_p}{\omega_0 L}$$

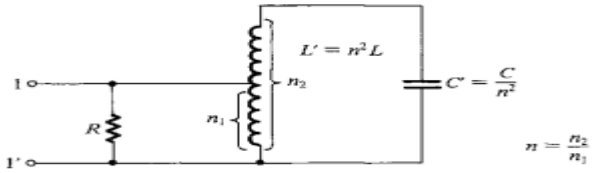
Equivalently

$$R_p = \omega_0 L Q_0$$

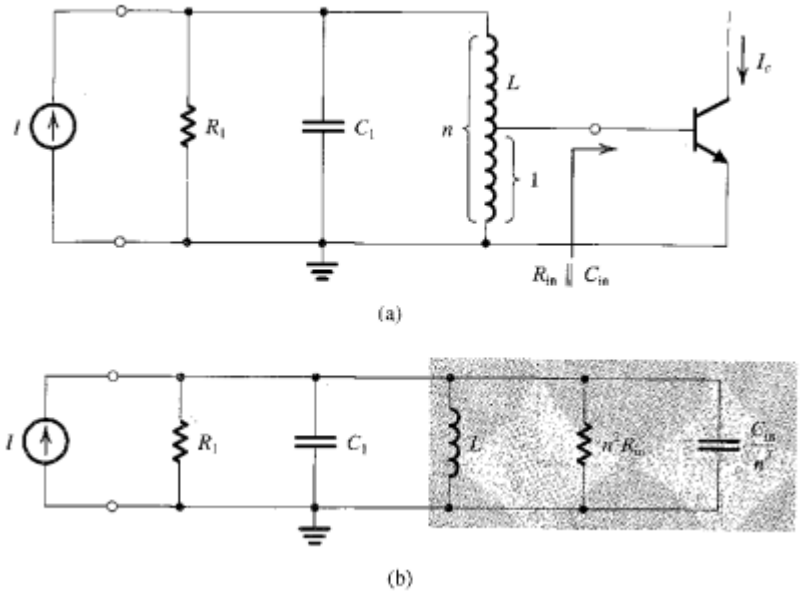
Use of Transformers:

In many cases it is found that the required value of inductance is not practical, in the sense that coils with the required inductance might not b e available with the required high values of Q_0. A simple solution is to use a transformer to effect an impedance change. Alternatively, a tapped coil, known as an autotransformer, can be used, as shown . Provided the two parts of the inductor are tightly coupled, which can b e achieved by winding on a ferrite core, the transformation relationships shown hold. The result is that the tuned circuit seen between terminals 1 and 1' is equivalent to .

In applications that involve coupling the output of a tuned amplifier to the input of another amplifier, the tapped coil can be used to raise the effective input resistance of the latter amplifier stage. In this way, one can avoid reduction of the overall Q. This point is illustrated in Fig.5 and in the following exercises.



A tapped inductor is used as an impedance transformer to allow using a higher inductance, L' and a smaller capacitance, C'



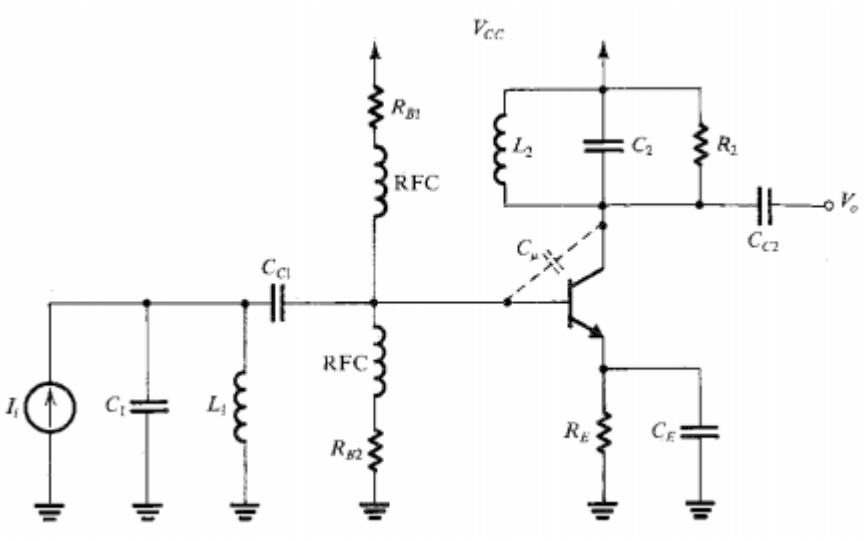
(a) The output of a tuned amplifier is coupled to the input of another amplifier via a tapped coil, (b) An equivalent circuit. Note that the use of a tapped coil increases the effective input impedance of the second amplifier stage.

Amplifiers with Multiple Tuned Circuits:

The selectivity achieved with the single-tuned circuit of below figure is not sufficient in many applications—for instance, in the IF amplifier of a radio or a TV receiver. Greater selectivity is obtained by using additional tuned stages. Figure shows a BJT with tuned circuits at both the input and the output. In this circuit the bias details are shown, from which we note that biasing is quite similar to the classical arrangement employed in low-frequency discrete-circuit design. However, to avoid the loading effect of the bias resistors R_m and RB_2 on the input tuned circuit, a radio-frequency choke (RFC) is inserted in series with each resistor. Such chokes have high impedances at the frequencies of interest. The use of RFCs in biasing tuned RF amplifiers is common practice.

The analysis and design of the double-tuned amplifier of Fig is complicated by the Miller effect 1 2 due to capacitance Since the load is not simply resistive, as was s the case in the amplifiers, the Miller impedance e at the input will be complex. This reflected impedance will cause detuning of the input circuit as well as "skewing" of the response of the input circuit. Needless to say, the coupling introduced by Cμ makes tuning (or aligning) the amplifier quite difficult. Worse e still, the capacitor Cμ can cause oscillations to occur and methods exist for neutralizing the effect of Cμ using additional circuits arranged to feed back a current equal and opposite to that through Cμ. An alternative, and preferred, approach is to use circuit configurations that do not suffer from the Miller effect. These are discussed later. Before leaving this section, however, we wish to point out that circuits of the type shown in Fig. 12.43 are usually designed utilizing the y-parameter mode l of the BJT. This is done because here, in view of the fact that C M plays a significant role, the y-parameter mode l makes s the analysis simpler (in comparison to that using the hybrid-π model). Also, the y

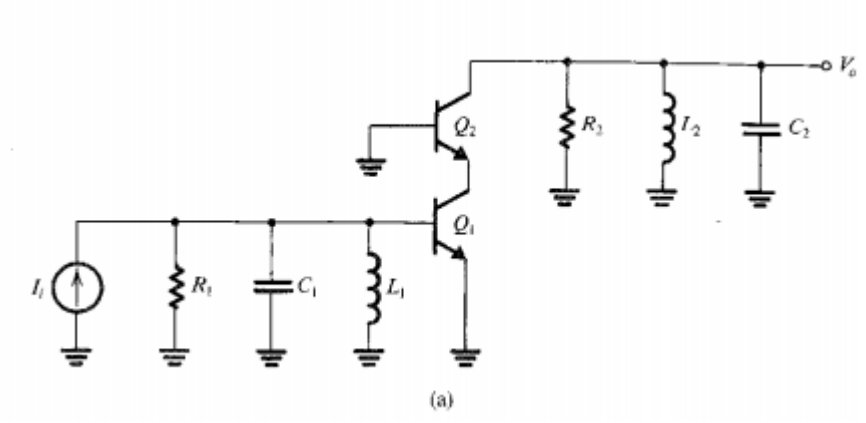
parameters can easily be measured at the particular frequency of interest W_0. For narrow-band amplifiers, the assumption is usually mad e that the y parameters remain approximately constant over the pass band.

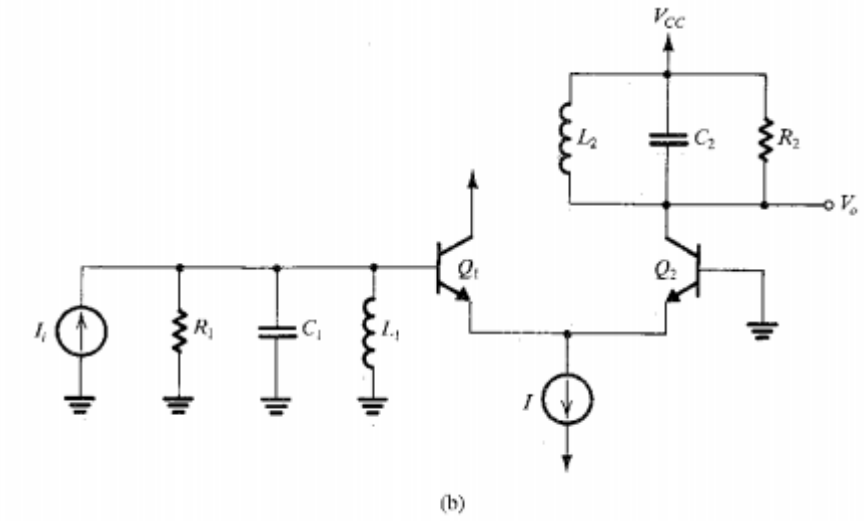


A BJT amplifier with tuned circuits at the input and the output.

The Cascode and the CC-CB Cascade:

We know that two amplifier configurations do not suffer from the Miller effect. These e are the cascode configuration and the common-collector common-bas e cascade. Figure shows tuned amplifiers based on these two configurations. The CC-CB cascade is usually preferred in IC implementations because its differential structure makes s it suitable for IC biasing techniques. (Note that the biasing details of the cascode circuit are not shown in Fig.





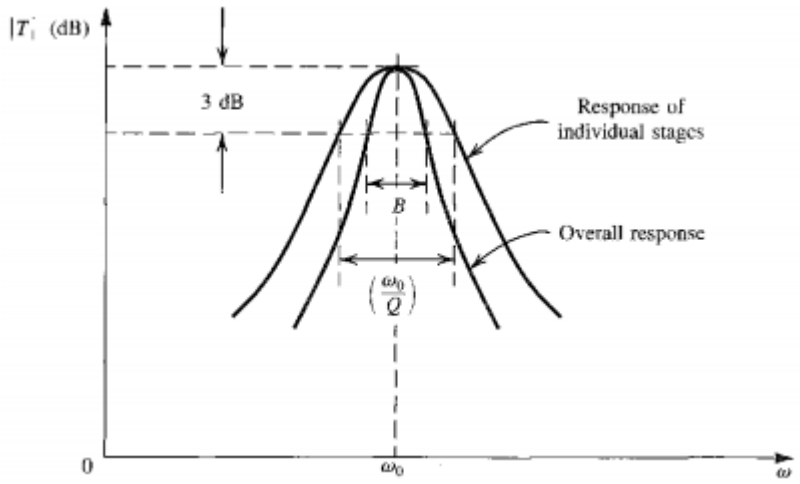
Two tuned-amplifier configurations that do not suffer from the Miller effect: (a) cascode and (b) common-collector common-base cascade.

Synchronous Tuning:

In the design of a tuned amplifier with multiple tuned circuits the question of the frequency to which each circuit should be tuned arises. The objective, of course, is for the overall response to exhibit high pass band flatness and skirt selectivity. To investigate this question, we shall assume that the overall response is the product of the individual responses: in other words, that the stages do not interact.

Consider first the case of N identical resonant circuits, known as the synchronously tuned case. Figure8 shows the response of an individual stage and that of the cascade. Observe the bandwidth "shrinkage" of the overall response. The 3-dB bandwidth B of the overall amplifier is related to that of the individual tuned circuits, W_0/Q is

$B = \frac{\omega_0}{Q}\sqrt{2^{1/N} - 1}$ where $\sqrt{2^{1/N} - 1}$ is known as the bandwidth-shrinkage factor.



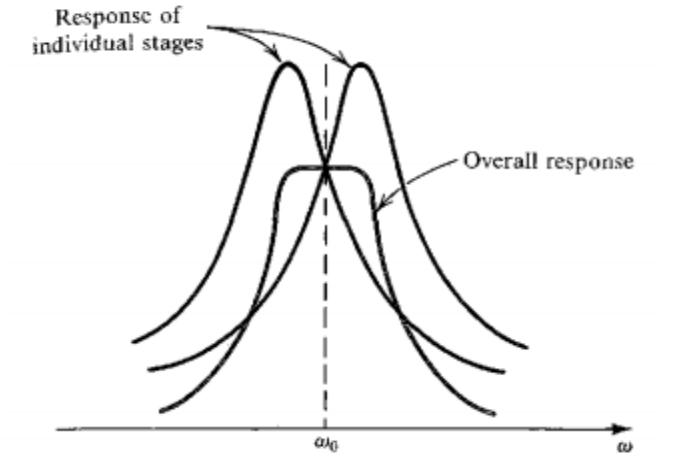
Frequency response of a synchronously tuned amplifier.

Stagger-Tuning:

A much better overall response is obtained by stagger-tuning the individual stages, as illustrated in Fig.. Stagger-tuned amplifiers are usually designed so that the overall response

exhibits maximal flatness around the center frequency f_0. Such a response can b e obtained by transforming the response of a maximally flat (Butterworth) low-pass filter up the frequency axis to W_0. We show here how this can be done. The transfer function of a second-order band pass filter can be expressed in terms of its poles as

$$T(s) = \frac{a_1 s}{\left(s + \frac{\omega_0}{2Q} - j\omega_0\sqrt{1 - \frac{1}{4Q^2}}\right)\left(s + \frac{\omega_0}{2Q} + j\omega_0\sqrt{1 - \frac{1}{4Q^2}}\right)}$$



Stagger-tuning the individual resonant circuits can result in an overall response with a pass band flatter than that obtained with synchronous tuning

UNIT-IV

Assignment-Cum-Tutorial Questions

A. Objective Questions

1) An op-amp is a _____ amplifier [ ]

A) High gain differential B) low gain differential

C) Moderate gain differential D) unity gain

2) Draw the schematic symbol of an op-amp.

3) Draw the equivalent symbol of an op-amp and indicate all the parameters.

4) The common-mode rejection ratio of an ideal op-amp is [ ]

A) very high B) Infinity C) always unity D) unpredictable

6) The differential gain of an op-amp is [ ]

A) very high B) very low C) dependent on input voltage D) about 100

7) The total output offset voltage is given by _____

8) The output of a particular op-amp increases 8V in 12μs. The slew rate is [ ]

A) 90 V/μs B) 0.67 V/μs C) 1.5 V/μs D) none of these

9) The input offset current equals the [ ]

A) difference between two base currents B) average of two base currents

C) collector current divided by current gain D) none of these

10) The output resistance of an ideal operational amplifier is [ ]

A) Infinity B) Low C) Very low D) Zero

11. **A tuned amplifier uses ..... Load**

12.For frequencies above the resonant frequency, a parallel LC circuit behaves as a ..... load

13.**For frequencies below resonant frequency, a series LC circuit behaves as a ..... load**

14.What is the relation between Bandwidth of synchronous tuned amplifier and individual tuned amplifier?

15.Neutralizing capacitor is connected between input and output nodes, to cancel out the effect of ..... Feedback

16. What is the reason for instability in Tuned amplifiers?

17. The selectivity of the tuned amplifier increases with Q factor (T/F)

18. What is the relation between Q and series internal resistance of an inductor r_s.

B. Subjective Questions

1. List out the ideal and practical specifications of an op-amp?
2. Define the following parameters with respect to op-amp

   A)Input bias current B) Input offset current C) Input offset voltage D) Slew rate
3. Identify why the input stage of an op-amp is DIBO differential amplifier.
4. Identify what can be the maximum gain of op-amp with the slew rate of 0.3V/μs when the input signal to op-amp is 0.03 sin $2x10^5t$.
5. If the response to a square wave input, the output of an op-amp changes from -12v to +12v over a time interval of 0.5μs identify the slew of the op-amp?
6. How fast can the output of op-amp change by 15v if its slew rate is 0.5v/μs?
7. Explain the inverting configuration under i) The closed loop gain ii)Effect of finite open loop gain iii) input and output resistance
8. Explain the Non inverting configuration under i) The closed loop gain ii)Effect of finite open loop gain

9. Briefly explain how op-amp will act as the Voltage follower

10. Explain the basic principle of Tuned Amplifiers.
11. Derive the expression for centre frequency and quality factor of a tuned Amplifier.
12. Explain about different types of tuned Amplifiers.
13. Discuss about the stability techniques in tuned amplifiers.

14. Explain briefly about Synchronous and stagger tuning

C. Previous GATE Questions

1) The ideal OP-AMP has the following characteristics GATE 2001

a. $R_i = \infty$, $A_V = \infty$, $R_o = 0$
b. $R_i = 0$, $A_V = \infty$, $R_o = 0$
c. $R_i = \infty$, $A_V = \infty$, $R_o = \infty$
d. $R_i = 0$, $A_V = \infty$, $R_o = \infty$

Answer: A

2) An ideal OP-AMP is an ideal

a. Voltage Controlled Current Source
b. Voltage Controlled Voltage Source
c. Current Controlled Current Source
d. Current Controlled Voltage Source

Answer: B

GATE 2004

3) If the differential voltage gain and the common mode voltage gain of a differential amplifier are 48 dB and 2 dB respectively, then common mode rejection ratio is

a. 23 dB
b. 25 dB
c. 46 dB
d. 50 dB

Answer: C

1) An amplifier using an op-amp with slewrate 1v/μs has a gain of 40Db. If this amplifier has to faithfully amplify sinusoidal signals from dc to 20 KHz without any slewrate introduced distortion, then the input signal level must not exceed----

a) 795mv b) 395mv c) 79.5 mv d) 39.5mv

2) A 741 opamp has again banwidth produt of 1MHz. A non-inverting amplifier using this op-amp and having a voltage gain of 20 dB will exhibit a -3dB bandwidth of -------

a) 50KHz b) 100KHz c) 100/17KHz d) 1000/7.07KHz

UNIT-V
FEEDBACK AMPLIFIERS

The concept of feedback involves feeding a small fraction of output at input by providing a connection from output to input. It is useful in several different ways in the design of amplifiers like stabilizing the gain, adjusting their impedances etc. and even to convert them into oscillators.

A classification of amplifiers, along with their ideal impedance characteristics is given. The concept of feedback, both positive and negative, is introduced and its impact on gain of the amplier is investigated. Different types of sampling and mixing are introduced along with their impact on the impedances of the amplifiers. Several amplifier circuits which use feedback for benefit are given.

5.1. Classification of amplifiers

There are several amplifiers and they are classified in different ways, depending upon different basis. According to one classification, amplifiers are divided into four types, namely, voltage amplifiers, current amplifiers, transresistance amplifiers and transconductance amplifiers. This classification is based on magnitudes of input and output impedances of amplifier relative to the source and load impedances, respectively.

The equivalent circuits of these four types of amplifiers, called models, are given and explained. These models use special kinds of sources, called dependent or controlled voltage and current sources. Each one is described briefly hereunder.

Voltage amplifier: By definition, voltage amplifier is one which provides a voltage output, V_o that is proportional to source voltage, V_s i.e.

$$V_o = A_v V_s \tag{5.1}$$

The proportionality factor, called voltage gain and indicated by A_v, should be independent of the magnitudes of the source and load resistances, R_s and R_L, respectively. But in practice A_v is dependent on R_s and R_L, and hence the gain provided by the amplifier varies with source and load conditions. Mathematically, the amplifiers operation can be described by,

$$V_o \approx A_v V_i \approx A_v V_s \tag{5.2}$$

Here, V_i is input voltage. One can notice that the voltage amplifier model uses voltage controlled voltage source. The model circuit of this amplifier is shown in Figure 5.1(a). For the voltage amplifier to be ideal i.e. to have A_v independent of R_s and R_L, its input resistance R_i should be infinite and output resistance R_o should be zero. In practice, infinite or zero values for these resistances are not realizable. However, by setting $R_i >> R_s$ and $R_o << R_L$ the behavior of voltage amplifier an be made approaching that of an ideal one.

Current amplifier: Current amplifier, by definition, is one which provides a load current I_L that is proportional to source current I_s i.e.

$$I_L = A_i I_s \tag{5.3}$$

The proportionality factor, called current gain and indicated by A_i, should be independent of the magnitudes of the source and load resistances, R_s and R_L, respectively. The model circuit of this amplifier is shown in Figure 5.1(b). But in practice A_i is dependent on R_s and R_L, and hence the gain provided by the amplifier varies with source and load conditions. Mathematically, the amplifiers operation can be described by,

$$I_L \approx A_i I_i \approx A_i I_s \tag{5.4}$$

Here, I_i is input current. One can notice that the current amplifier model uses current controlled current source. For current amplifier to be ideal i.e. to have A_i independent of R_s and R_L, its input resistance R_i should be zero and output resistance R_o should be infinity. In practice, zero or infinite values for these resistances are not realizable, and hence, an ideal amplifier can never be realiezed. However, by setting $R_i << R_s$ and $R_o >> R_L$, the behavior of current amplifier can be made approaching that of an ideal one.

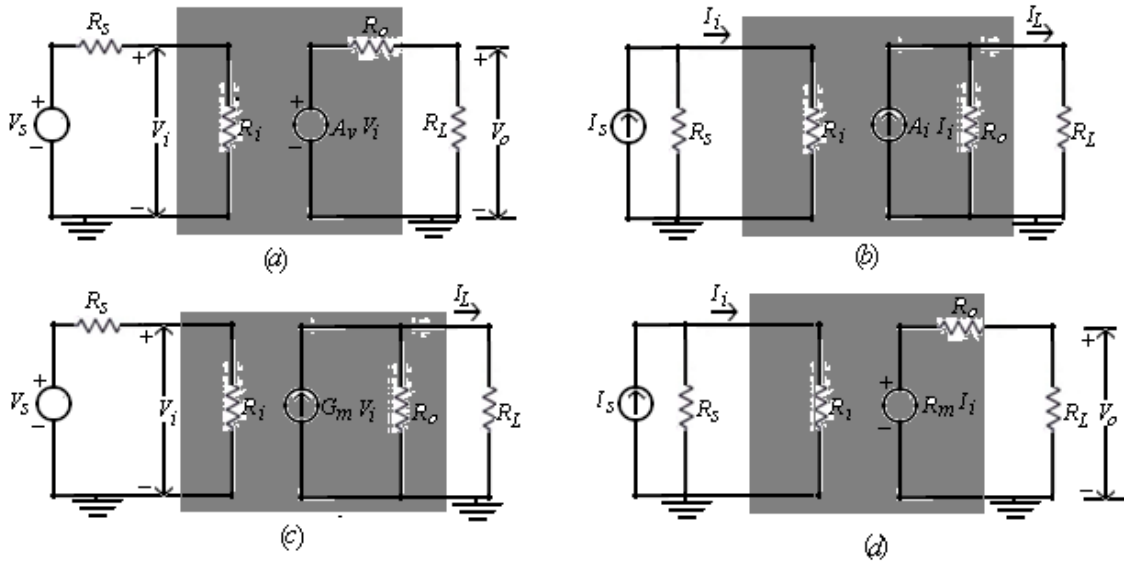


Figure 5.1 Equivalent circuit of (a) voltage amplifier, (b) current amplifier, (c) transconductance amplifier and (d) transresistance amplifier

Transconductance amplifier: By definition, transconductance amplifier is one which provides a load current I_L that is proportional to source voltage V_s i.e.

$$I_L = G_m V_s \qquad (5.5)$$

The proportionality factor, called transconductance and indicated by G_m, should be independent of the magnitudes of the source and load resistances, R_s and R_L, respectively. The model circuit of this amplifier is shown in Figure 5.1(c). In practice G_m is dependent on R_s and R_L, and hence, transconductance provided by the amplifier varies with source and load conditions. Mathematically, the amplifiers operation can be described by,

$$I_L \approx G_m V_i \approx G_m V_s \qquad (5.6)$$

Here, V_i is input voltage. One can notice that transconductance amplifier model uses voltage controlled current source. For transconductance amplifier to be ideal i.e. to have G_m independent of R_s and R_L, its input resistance R_i as well output resistance R_o should be infinity. In practice, infinite values for these resistances are not realizable. However, by setting $R_i >> R_s$ and $R_o >> R_L$ the behavior of transconductance amplifier can be made approaching that of an ideal one.

Transresistance amplifier: By definition, transresistance amplifier is one which provides a voltage output V_o that is proportional to source current I_s i.e.

$$V_o = R_m I_s \qquad (5.7)$$

The proportionality factor, called transresistance and indicated by R_m, should be independent of the magnitudes of the source and load resistances, R_s and R_L, respectively. The model circuit of this amplifier is shown in Figure 5.1(d). In practice R_m is dependent on R_s and R_L, and hence, transresistance provided by the amplifier varies with source and load conditions. Mathematically, the amplifiers operation can be described by,

$$V_o \approx R_m I_i \approx R_m I_s \qquad (5.8)$$

Here, I_i is input current. One can notice that transresistance amplifier model uses voltage controlled current source. For transresistance amplifier to be ideal i.e. to have R_m independent of R_s and R_L, its input resistance R_i as well output resistance R_o should be zero. In practice, zero values for these

resistances are not realizable. However, by setting $R_i << R_s$ and $R_o << R_L$ the behavior of transresistance amplifier can be made approaching that of an ideal one.

Table 1 Ideal characteristics of amplifiers.

S.No	Amplifier attribute	Voltage amplifier	Current amplifier	Transconductance amplifier	Transresistance amplifier
1.	R_i	∞	0	∞	0
2.	R_o	0	∞	∞	0
3.	Transfer characteristic	$V_o=A_vV_s$	$I_L=A_iI_s$	$I_L=G_mV_s$	$V_o=R_mI_s$

It can be observed, in general, that the input and output resistances require to be high and low for voltage amplifiers, low and high for current amplifiers, low and low for transresistance amplifiers, high and high for transconductance amplifiers. Otherwise, the transfer gain of the amplifier becomes dependent upon the source as well as the load resistances. For example, the gain of the voltage amplifier can be expressed as,

$$A_{VS} = \frac{V_o}{V_s} = \frac{A_v V_i R_L}{(R_o + R_L)V_s} = A_v \frac{R_L}{(R_o + R_L)} \frac{R_i}{(R_s + R_i)} \qquad (5.9)$$

It can be noticed from the above expression that the voltage gain is dependent upon the source as well as the load resistances. Hence, this amplifier offers different amounts of gain in different circuits, depending upon the prevailing source and load resistances, which is really a drawback. It can also be observed that voltage gain becomes independent of source resistance if the input resistance is infinity or comparatively large with respect to source resistance. Similarly, the gain becomes independent of load resistance if the output resistance is zero, or comparatively small with respect to load resistance. Therefore, it is sufficient for a voltage amplifier to have high input and low output resistances for the sake of stabilized or fixed voltage gain. With similar reasoning applied to other types of amplifiers one can find out the requirements on their input and output resistances for giving fixed gains.

Applying feedback in proper configuration, it is possible to set the input and output resistances of the amplifiers at the required level, and have fixed amount of gain. However, one has to pay a price for the benefit of stabilized gain: the maximum realizable gain from the amplifier comes down.

5.2. Single loop feed back amplifier

Feedback is a technique in which the output signal is brought to the input side, mixed with the external signal and then the combined signal is given as input to the basic amplifier. Two types of feedback systems are there: widely used negative feedback, which reduces the gain when applied to amplifiers, and positive feedback used in the design of oscillators. With the application of negative feedback to amplifiers, two important changes take place.

1. The transfer gain gets desensitized i.e. dependence on the active circuit parameters, temperature and aging gets decreased, a desirable feature.
2. The transfer gain gets decreased, always unwanted.

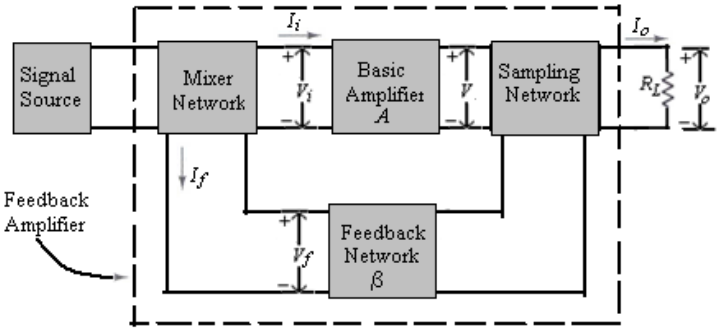


Figure 5.2 Illustrating its basic components of single-loop feedback system.

A single-loop feedback system, shown in Figure 5.2, consists of basically the following elements:

1. Signal source: the signal source can be represented either by Thevenin's or by Norton's representation. But it convenient for manipulation to denote the source by Thevenin's voltage

source when the mixing is in series and by Norton's current source when the mixing is in shunt with the source.

2. Basic amplifier: It may belong to one of the four categories mentioned above. We go to feedback if its input or output resistance or both are not according to requirement. As an example we can consider BJT CB voltage amplifier whose input and output resistances are required to be high and low whereas in practice they are low and high. By applying appropriate feedback(voltage series) it is possible to adjust the input and output resistance values of the above amplifier to the desired levels.
3. Feedback network: It is usually a passive two-port network consisting of resistors, inductors and capacitors. So its transfer function or feedback factor β is in general function of frequency, f i.e. $\beta(f)$. In case of voltage sampling its input is voltage and in the case of current sampling it is current. For series mixing its output voltage is taken as feedback signal and in case of shunt mixing its output current is taken as feedback signal.

Comparator or mixer: The input resistance of an amplifier can be varied by selecting appropriate mixer circuit. Basically there are two types of mixers: series mixers and shunt mixers, as shown in Figure 5.3. We explain about each one of them and discuss their applications.

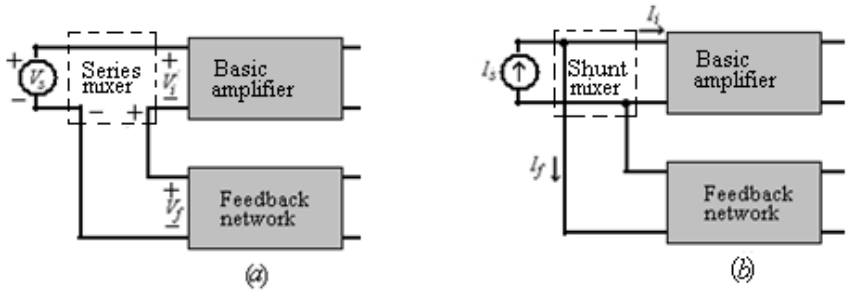


Figure 5.3 Input side feedback connections of a basic amplifier (a) Series comparion and (b) shunt comparison.

(i) *Series or loop mixer*: In this type of mixing, the feedback signal is connected in series with the input signal source. The feedback signal is necessarily a voltage and this type of mixing, you are going to see, increases the input resistance of the amplifier.

As shown in Figure 5.4(a), The input resistance of the amplifier in the absence of the feedback is

$$R_i = \frac{V_s}{I_i} = \frac{V_i}{I_i} \qquad (5.10)$$

The input resistance of the amplifier with feedback is

$$R_{if} = \frac{V_s}{I_i} = \frac{V_i + V_f}{I_i} \qquad (5.11)$$

The denominators of the both the quantities are same. However, numerators are not same and in the expression of resistance with feedback it is large. Now, it is obvious that the series mixing increases the input resistance of the amplifier.

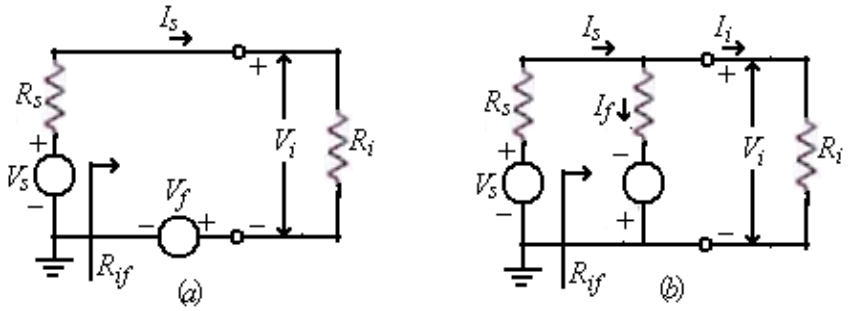


Figure 5.4 Input resistance affected by mixer connections.(a) Series connection and (b) shunt connection.

(ii) *Shunt or node mixer*: In this type of mixing, shown in Figure 5.3(b), the feedback signal is connected in shunt with the input signal source. The feedback signal is necessarily a current and this type of mixing decreases the input resistance of the amplifier.

As shown in Figure 5.4(b), the input resistance of the amplifier in the absence of the feedback is

$$R_i = \frac{V_s}{I_i} = \frac{V_i}{I_i} \tag{5.12}$$

The input resistance of the amplifier with feedback is

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f} \tag{5.13}$$

The numerators of the both the quantities are same. However, denominators are not same and in the expression of resistance with feedback, it is large. Therefore, we can conclude that the shunt mixing decreases the input resistance of the amplifier.

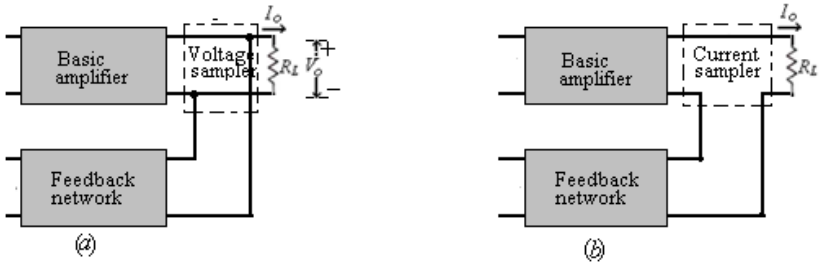


Figure 5.5 Output side feedback connections of a basic amplifier (a) Voltage sampling and (b) current sampling.

4. **Sampler**: The output resistance of an amplifier can be varied by selecting appropriate sampler circuit. Basically there are two types of samplers: voltage samplers and current samplers, as shown in Figure 5.5. We discuss about both the types of samplers here and try to understand their impact on the out put resistances of the amplifiers.

(i) *Voltage or node sampling*: In this type of sampling the sampled signal is the voltage across the load. So the sampled signal is necessarily a voltage and this type of sampling decreases the output resistance of the amplifier. The output resistance of the amplifier in the absence of the feedback is

$$R_o = \frac{V}{I} \tag{5.14}$$

The output resistance of the amplifier with feedback is

$$R_{of} = \frac{V}{I + I'_f} \tag{5.15}$$

The numerators of the both the quantities are same. However, denominators are not same and in the expression of resistance with feedback, it is large. It is obvious that the voltage sampling decreases the output resistance of the amplifier.

(ii) *Current or loop sampling*: In this type of sampling the current through the load is sampled. So in this case the sampled signal is current and this type of sampling is useful to increase the output resistance of the amplifier. The output resistance of the amplifier in the absence of the feedback is

$$R_o = \frac{V}{I} \tag{5.16}$$

The output resistance of the amplifier with feedback is

$$R_{of} = \frac{V + V'_f}{I} \tag{5.17}$$

The denominators of the both the quantities are same. However, numerators are not same and in the expression of resistance with feedback it is large. Therefore it is obvious that the current sampling increases the input resistance of the amplifier.

5.3. Feedback specifications

Here is given frequently used terminology in feedback theory along with their meanings, definitions and expressions.

1. **Loop gain** or **return ratio:** The product $-\beta A$ is called the loop gain or return ratio.

2. **Return difference or de-sensitivity** The difference between unity and the loop gain is called the return difference. $D=1+\beta A$.
3. **Amount of feedback** The amount of feedback in decibels is

$$N = \text{dB of feedback} = 20\log\left|\frac{A_f}{A}\right| = 20\log\left|\frac{1}{1+A\beta}\right|. \qquad (5.18)$$

For negative feedback, it is a negative number.

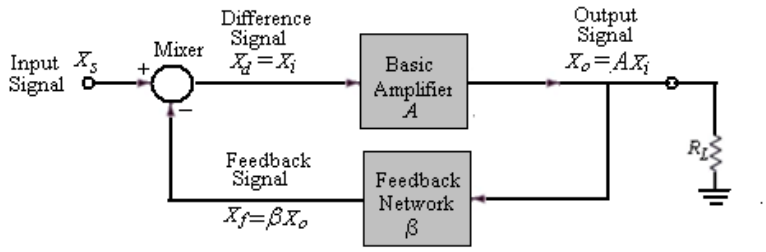


Figure 5.6 Illustrating schematic representation of a single-loop feedback system.

4. **Transfer gain with negative feedback :**
With the application of the negative feedback, the gain of the amplifier decreases. An expression for the reduced gain can be derived as follows: With reference to Figure 5.6, the output signal can be written that,

$$X_o = AX_i = AX_d = A\left(X_s - X_f\right) = A\left(X_s - \beta X_o\right)$$

$$X_o + \beta AX_o = AX_s \text{ or } X_o\left(1+\beta A\right) = AX_s$$

The transfer gain of the amplifier with feedback by definition then is

$$A_f \equiv \frac{X_o}{X_s} = \frac{A}{\left(1+\beta A\right)} \qquad (5.19)$$

One can easily notice that the gain of amplifier, with feedback, is less than that without feedback. Also this relation is independent of type of mixing as well as sampling i.e. it holds good for all the four types of configurations.

While deriving the expression above, the following fundamental assumptions of feedback amplifiers are made:

- The input signal is transmitted to the output through the amplifier A and not through the feedback network.
- The output signal is transmitted to the input through the β network and not through the amplifier, A.
- The reverse transmission factor β of the feedback network is independent of the load and the source resistances R_L and R_s.

5. **Sensitivity** It is defined as the fractional change in amplification with feedback dA_f/A_f divided by the fractional change without feed back dA/A is called the sensitivity of the transfer gain. Differentiating the expression for gain from Eq. (5.19), it can be found that,

$$A_f = \frac{A}{\left(1+\beta A\right)} \rightarrow dA_f = \frac{dA}{\left(1+\beta A\right)} - \frac{\beta A dA}{\left(1+\beta A\right)^2}$$

$$dA_f = dA\left[\frac{1}{\left(1+\beta A\right)} - \frac{\beta A}{\left(1+\beta A\right)^2}\right] = dA\left[\frac{\left(1+\beta A\right)-\beta A}{\left(1+\beta A\right)^2}\right] = \frac{dA}{\left(1+\beta A\right)^2}$$

$$\frac{dA_f}{A_f} = \frac{dA}{\left(1+\beta A\right)^2}\frac{\left(1+\beta A\right)}{A} = \frac{1}{\left(1+\beta A\right)}\frac{dA}{A}$$

Therefore, the sensitivity is

$$\frac{dA_f/A_f}{dA/A} = \frac{1}{(1+\beta A)} \qquad (5.20)$$

5.4. Negative feedback

When any increase in the output signal results in a feedback signal into the input in such a way as to cause a decrease in the output signal, the amplifier is said to have negative feedback.

Advantages: When applied to amplifiers, the negative feedback has the following two primary applications.

- Any of the four basic types of amplifiers may be improved by the proper use of the negative feedback.
- Negative feedback improves the frequency response and linearity of the amplifiers significantly.

Disadvantages: The amplifiers suffer on the following two conunts because of negative feedback.

- The gain of the amplifier gets reduced with the application of negative feedback.
- Negative feedback may result in instability and oscillations in the system.

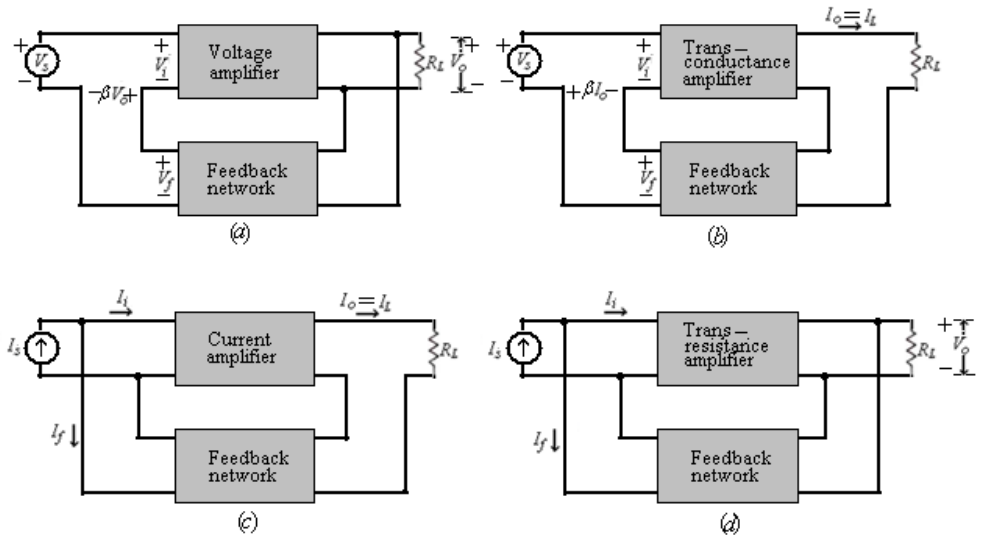


Figure 5.7 Topologies of feedback amplifiers, considering the source resistance as part of the amplifier. (a) Voltage-series feedback applied to voltage amplifier (b) current-series feedback applied to transconductance amplifier (c) Current-shunt feedback applied to current amplifier (d) Voltage-shunt feedback applied to transresistance amplifier.

General characteristics of negative feedback

Different topologies of feedback amplifiers are shown in Figure 5.7. Here, the characteristics and impact of negative feedback on amplifiers are considered and explained.

1. **Transfer gain with negative feedback**

   It has been found earlier an expression for gain of feedback amplifier in terms of gain without feedback. From the expression, it has also been noticed that the gain of amplifier, with feedback, is less than that without feedback, independent of type of mixing as well as sampling.

2. **De-sensitivity of transfer amplification** If the feedback network contains only stable passive elements, a substantial improvement in stability can be achieved.

   Voltage- series feedback stabilizes voltage gain, A_{Vf}

   Current- series feedback stabilizes transconductance, G_{Mf}

   Current-shunt feedback stabilizes current gain, A_{If}

   Voltage-shunt feedback stabilizes transresistance, R_{Mf}

Table 5.2 Impact of negative feedback on amplifier performance.

S.No.	Attribute	Voltage- series feedback	Current-series feedback	Current-shunt feedback	Voltage-shunt feedback
1.	R_{of}	Decrease	Increase	Increase	Decrease

2.	R_{if}	Increase	Increase	Decrease	Decrease
3.	Improved characteristic	Voltage amplifier	Transconductance amplifier	Current amplifier	Transresistance amplifier
4.	Desensitizes	A_{Vf}	G_{Mf}	A_{If}	R_{Mf}
5.	Bandwidth	Increase	Increase	Increase	Increase
6.	Nonlinear distortion	Decrease	Decrease	Decrease	Decrease

7. **Frequency distortion** If the feedback network does not contain reactive elements, the overall gain is not a function of frequency. Under these circumstances a substantial reduction in frequency and phase distortion is obtained.
8. **Non linear distortion** The harmonics generated due to nonlinearity in the amplifier gets divided by factor *D* if the feedback is employed.
9. **Reduction of noise** It can be shown that the noise introduced in an amplifier is divided by the factor *D* if the feedback is employed. If the additional gain required to compensate what is lost because of the presence of inverse feedback can be obtained by a readjustment of the circuit parameters rather than by the addition of extra stage, a definite reduction will result from the presence of the feedback. In particular, the hum introduced into the circuit by a poorly filtered power supply may be decreased appreciably.

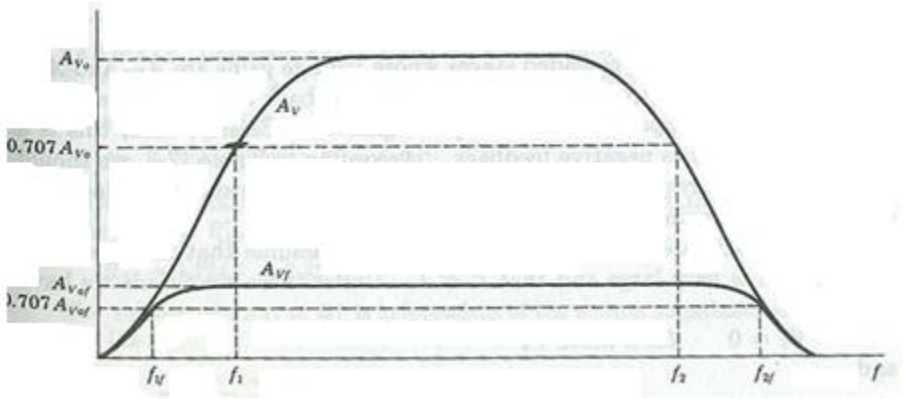


Figure 5.8 Illustraing the decrease in voltage gain and increae in bandwidth for an amplifier when voltage-series feedback is applied.

10. **Bandwidth improvement** The bandwidth increases by a factor which is equal to the factor by which the gain decreases, as shown in Figure 5.8. The midband amplification with feedback A_{of} equals to the midband amplification without feedback A_o divided by 1+ βA_o. The high 3dB frequency with feedback f_{Hf} equals the corresponding 3dB frequency without feedback f_H multiplied by the same factor 1+ βA_o. Also the low 3dB frequency with feedback f_{Lf} equals the corresponding 3dB frequency without feedback f_L decreased by the same factor 1+ βA_o . For an audio or video amplifier, $f_H >> f_L$ and hence the band width is $f_H - f_L \approx f_H$. Under these circumstances, one can observe that the gain bandwidth product is the same with or without feedback.

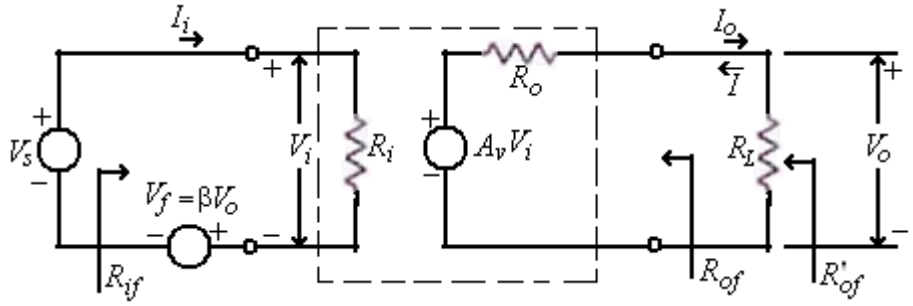
5.5. Analysis of amplifiers with feedback

Here, the input resistance and low output resistances various amplifires with feedback applied are discussed and expressions for them are derived.

5.5.1 Voltage amplifier with feedback

For the sake of gain stabilization, that is to make the voltage gain independent of the source and load resistances, the voltage amplifier requires to have high input resistance and low output resistance. So the mixing should be of such a type which can increase the input resistance i.e. series whereas the sampling should be able to decrease the output resistance i.e. voltage. Therefore it is the voltage-series configuration that can be used with the feedback of the voltage amplifiers.

Figure 5.10 A voltage amplifier with voltage-series feedback applied.



Input resistance: By definition, the input resistance with feedback is,

$$R_{if} \equiv \frac{V_s}{I_i} \tag{5.21}$$

From the input circuit, the source voltage can be expressed as,

$$V_s = I_i R_i + V_f = I_i R_i + \beta V_o \tag{5.22}$$

From the output circuit, the output voltage can be written that,

$$V_o = \frac{A_v V_i R_L}{R_o + R_L} = A_V I_i R_i \tag{5.23}$$

where A_V is voltge gain, given by,

$$A_V \equiv \frac{V_o}{V_i} = \frac{A_v R_L}{R_o + R_L}.$$

Combining Eqs. (5.22) and (5.23), the ratio of V_s to I_i that is R_{if} can be found as,

$$R_{if} = \frac{V_s}{I_i} = R_i \left(1 + \beta A_V\right) \tag{5.24}$$

Note that, the voltage gain A_v represents the open-circuit gain, where as the voltage gain A_V is the gain after taking the load R_L into account, both, without feedback. Hence, one is related to other through,

$$A_v = \lim_{R_L \to \infty} A_V \tag{5.25}$$

Note: In the above analysis, the source resistance has not been taken into account. In the case of series mixing, the input resistance usually rises to high values and when compared to it, the source resistance becomes small. As a consequence, the presence or absence of the source resistance in the input circuit does not make any significant difference in the analysis of the amplifier and hence we neglected it.

Output resistance: The output resistance with feedback R_{of} is the resistance at the output terminals of the amplifier but with load R_L disconnected. Finding the output resistance is a two-step procedure: in the first step remove the input signal source by with a short if it is voltage source and by a open circuit if it is a current source. Simultaneously set the output resistance to infinity by removing the terminating load R_L from the circuit. In the second step apply a voltage V across the output terminals and then find the current I driven by it into the circuit. The ratio voltage V to current I gives the output resistance of the amplifier. Hence,

$$R_{of} \equiv \frac{V}{I} \tag{5.26}$$

As $V_s = 0$, the input voltage can be written as,

$$V_i = -V_f = -\beta V \tag{5.27}$$

Using the Eq.(5.27), the current into the amplifier, from output side, can be written as,

$$I = \frac{V - A_v V_i}{R_o} = \frac{V + \beta A_v V}{R_o} \tag{5.28}$$

Hence, from Eq.(5.28), the ratio of V to I, that is output resistance R_{of} of the amplifier with feedback can be found as,

$$R_{of} \equiv \frac{V}{I} = \frac{R_0}{(1+\beta A_v)} \tag{5.29}$$

The output resistance with feedback R'_{of}, which includes R_L as part amplifier is given by R_{of} in parallel with R_L. Hence,

$$R'_{of} = R_{of} \parallel R_L = \frac{R'_0}{(1+\beta A_V)} \tag{5.30}$$

where

$$R'_o = R_o \parallel R_L = \frac{R_o R_L}{R_o + R_L} \tag{5.31}$$

Current amplifier with feedback:

For current gain stabilization, the input resistance requires to be low whereas the output resistance needs to be high in current amplifier. So the mixing and sampling should be of such a type which can decrease the input resistance and increase the output resistance. Therefore it is the current-shunt configuration that can be used with the feedback of the current amplifiers.

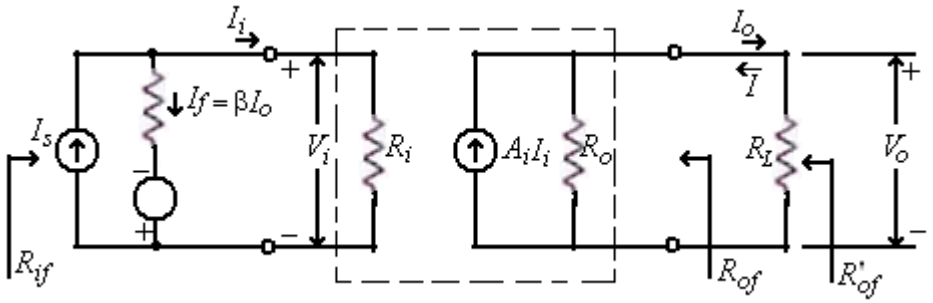


Figure 5.11 A current amplifier with current-shunt feedback applied.

Input resistance: From the input circuit of the amplifier, the source current can be written as,

$$I_s = I_i + I_f = I_i + \beta I_o. \tag{5.32}$$

From the output circuit, the output current can be written as,

$$I_o = \frac{A_i I_i R_o}{R_o + R_L} = A_I I_i \tag{5.33}$$

where A_I is current gain, given by,

$$A_I = \frac{A_i R_o}{R_o + R_L}$$

Using expression for output current available in Eq. (5.33) into Eq. (5.32), the source current can be expressed as,

$$I_s = I_i + I_f = I_i (1+\beta A_I) \tag{5.34}$$

Using expression for source current available in Eq. (5.34), the input resistance R_{if} with feedback can be found as,

$$R_{if} \equiv \frac{V_i}{I_s} = \frac{V_i}{(1+\beta A_I) I_i} = \frac{R_i}{(1+\beta A_I)} \tag{5.35}$$

Note that the gain A_i represents the short-circuit i.e. $R_L = 0$ current gain, where as the gain A_I is the current gain with the load R_L connected, both, without feedback. Hence, $A_i = \lim_{R_L \to 0} A_I$

(5.36)

Note: In the above analysis, we have not taken into account the source resistance. In the case of shunt mixing, the input resistance usually falls to small values and when compared to it, the source resistance becomes very large. As a consequence, the presence or absence of the source resistance in

the input circuit does not make any significant difference in the analysis of the amplifier and hence we neglected it.

Output resistance: To find the output resistance, R_{of} remove the external signal source and termination resistance. Now apply a voltage V across the output terminals and then find the current I driven by it into the circuit. The ratio of voltage V to current I gives the output resistance of the amplifier. Now, from the output circuit current into amplifier can be written as,

$$I = \frac{V}{R_o} - A_i I_i \qquad (5.35)$$

From the input circuit as $I_s = 0$, the input current can be expressed as,

$$I_i = -I_f = -\beta I_o = \beta I. \qquad (5.36)$$

Manipulating the relation available in Eq. (5.36), the ratio of V to I i.e.the output resistnace, R_{of} with feedback can be found as,

$$I = \frac{V}{R_o} - \beta A_i I$$

$$I\left(1+\beta A_i\right) = \frac{V}{R_o}$$

$$R_{of} \equiv \frac{V}{I} = R_0\left(1+\beta A_i\right) \qquad (5.37)$$

The output resistance with feedback, R'_{of} which includes R_L as part amplifier, is given by R_{of} in parallel with R_L .

$$R'_{of} = R_{of} \,\square\, R_L = \frac{R'_0\left(1+\beta A_i\right)}{\left(1+\beta A_I\right)} \qquad (5.38)$$

where

$$R'_o = R_o \,\square\, R_L = \frac{R_o R_L}{R_o + R_L} \qquad (5.39)$$

Transconductance amplifier with feedback:

For the stabilization of transconductance, both the input and output resistances requires to be high. The type of mixing that can increase the input resistance is series and the type of sampling that can increase the output resistance is current sampling. So the configuration that is suitable for the feedback of the transconductance amplifiers is the current-series.

Input resistance: The input impedance of the amplifier with feedback is ratio of source voltage to input current. From the input circuit, the source voltage can be written as,

$$V_s = I_i R_i + V_f = I_i R_i + \beta I_o \qquad (5.40)$$

But from the output circuit, the output current can be expressed as,

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = \frac{G_m I_i R_o R_i}{R_o + R_L} \qquad (5.41)$$

Combining Eqs.(5.40) and (5.41), the source voltage can be found as,

$$V_s = I_i R_i + \beta I_o = I_i R_i + \beta \frac{G_m I_i R_o R_i}{R_o + R_L} = I_i R_i \left(1+\frac{\beta G_m R_o}{R_o + R_L}\right) = I_i R_i\left(1+\beta G_M\right) \qquad (5.42)$$

From Eq. (5.42), the ratio V_s / I_i , that is the input resistance with feedback R_{if} can be found as,

$$R_{if} = \frac{V_s}{I_i} = R_i\left(1+\beta G_M\right) \qquad (5.43)$$

where G_M is transconductance given by,

$$G_M \equiv \frac{I_o}{V_i} = \frac{G_m R_o}{R_o + R_L} \qquad (5.44)$$

Note that, whereas G_m represents the short-circuit transconductance , the G_M is the transconductance without feedback after taking the load R_L into account. Thus,

$$G_m = \lim_{R_L \to 0} G_M \tag{5.45}$$

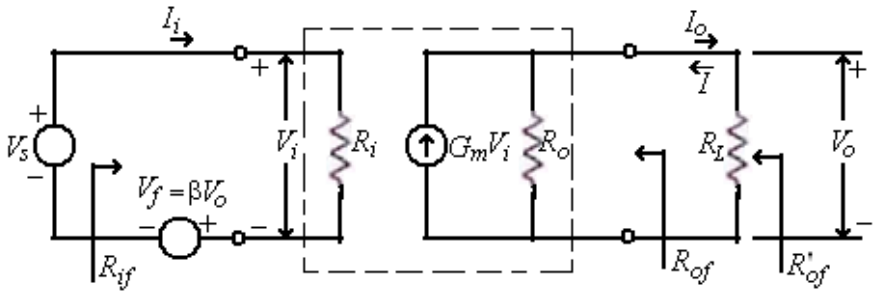


Figure 5.12 A transconductance amplifier with current-series feedback applied.

Output resistance: To find the output resistance with feedback remove the external signal source and replace the load resistance with a source of voltage V across the output terminals and then find the current I driven by it into the circuit. The ratio of voltage V to current I gives the output resistance of the amplifier. Now from the output circuit

$$I = \frac{V}{R_o} - G_m V_i \tag{5.46}$$

In the input circuit, as V_s =0, the input voltage V_i can be expressed as

$$V_i = -V_f = -\beta I_o = \beta I \,. \tag{5.47}$$

Combining Eqs.(5.46) and (5.47) and then solving for output resistance, R_{of} gives,

$$I = \frac{V}{R_o} - \beta G_m I \rightarrow I\left(1 + \beta G_m\right) = \frac{V}{R_o}$$

$$R_{of} \equiv \frac{V}{I} = R_0\left(1 + \beta G_m\right) \tag{5.48}$$

The output resistance with feedback, R'_{of} which includes R_L as part amplifier is given by R_{of} in parallel with R_L .

$$R'_{of} = R_{of} \,\square\, R_L = \frac{R'_0\left(1 + \beta G_m\right)}{\left(1 + \beta G_M\right)} \tag{5.49}$$

where $R'_o = R_o \,\square\, R_L$

Transresistance amplifier with feedback:

For transresistance stabilization, the input as well as the output resistances of the amplifier requires to be low. So we require using the type of mixing and sampling which can decrease the input and output resistances. The suitable configuration naturally will be current shunt for the transresistance amplifiers.

Input resistance: From the input circuit, the source current can be written as,

$$I_s = I_i + I_f = I_i + \beta V_o. \tag{5.50}$$

And from the output circuit, the output voltage can be expressed as,

$$V_o = \frac{R_m I_i R_L}{R_o + R_L} = R_M I_i \tag{5.51}$$

where R_M is transresistance, given by,

$$R_M = \frac{R_m R_L}{R_o + R_L} \tag{5.52}$$

Combining Eqs.(5.50) and (5.51), the source current can be written as,

$$I_s = I_i + \beta R_M I_i = I_i\left(1 + \beta R_M\right) \tag{5.53}$$

Solivng Eq. (5.53)for the ratio of input voltage to source current i.e. input resistance, results in,

$$R_{if} = \frac{V_i}{I_s} = \frac{R_i}{\left(1 + \beta R_M\right)} = \frac{V_i}{\left(1 + \beta R_M\right) I_i} = \frac{R_i}{\left(1 + \beta R_M\right)} \tag{5.54}$$

where

$$R_M \equiv \frac{V_o}{I_i} = \frac{R_m R_L}{R_o + R_L} \qquad (5.55)$$

Note that R_m represents the open-circuit transresistance, whereas the R_M is the transresistance when the termination is R_L .

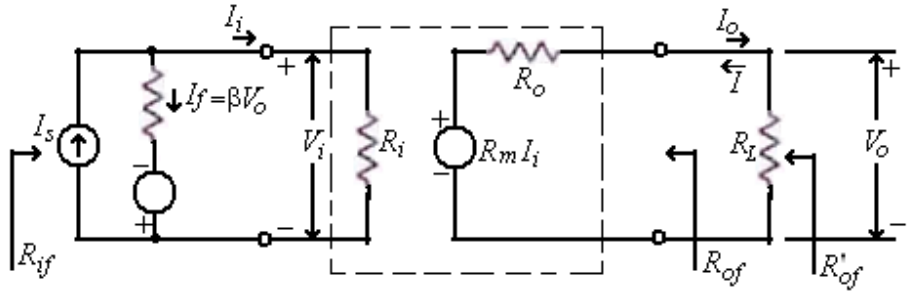


Figure 5.13 A transresistance amplifier with voltage-shunt feedback applied.

Output resistance: The resistance R_{of} is output resistance with feedback i.e. resistance seen when looking into output terminals without load R_L. If a voltage source V drives a current I into the output terminals of the amplifier in the absence of signal source and load resistance, then the output resistance becomes,

$$R_{of} \equiv \frac{V}{I}. \qquad (5.56)$$

For Series comparison $R_{if} > R_i$ **and for Shunt comparison** $R_{if} < R_i$

Series mixing	Shunt mixing
Voltage-series $R_{if} = R_i(1+\beta A_V)$	**Voltage-shunt** $R_{if} = \frac{R_i}{(1+\beta R_M)}$
Current-series $R_{if} = R_i(1+\beta G_M)$	**Current-shunt** $R_{if} = \frac{R_i}{(1+\beta A_I)}$

For Voltage sampling $R_{of} < R_o$ **and for Current sampling** $R_{of} > R_o$

Voltage sampling	Currrent sampling
Voltage-series $R'_{of} = \frac{R'_0}{(1+\beta A_V)}$	**Current-series** $R'_{of} = \frac{R'_0(1+\beta G_m)}{(1+\beta G_M)}$
Voltage-shunt $R'_{of} = \frac{R'_0}{(1+\beta R_M)}$	**Current-shunt** $R'_{of} = \frac{R'_0(1+\beta A_i)}{(1+\beta A_I)}$

The current into the amplifier from the output terminals can be expressed as,

$$I = \frac{V - R_m I_i}{R_o} \qquad (5.57)$$

From the input circuit, as $I_s = 0$, the input current can be found as,

$$I_i = -I_f = -\beta I_o = \beta I. \qquad (5.58)$$

Combining Eqs.(5.57) and (5.58), and then solving for V to I ratio, the output resistance can be established as,

$$I = \frac{V + \beta R_m I}{R_o}$$

$$R_{of} \equiv \frac{V}{I} = \frac{R_0}{(1+\beta R_m)} \qquad (5.59)$$

The output resistance, R'_{of} with feedback including R_L as part amplifier, is given by R_{of} in parallel with R_L .

$$R'_{of} = R_{of} \square R_L = \frac{R'_0}{(1+\beta R_M)} \qquad (5.60)$$

where $R'_o = R_o \square R_L$.

Here R'_o is output resistance without feedback but taking the load R_L into account. Therefore,

$$R_m = \lim_{R_L \to \infty} R_M \qquad (5.61)$$

5.6. Example circuits with feedback

5.6.1. Method of Analysis of a Feedback Amplifier

It is desirable to separate the feedback amplifier into two blocks, the basic amplifier A and the feedback network β, because with a knowledge of A and β, we can calculate the important characteristics of the feedback system, namely, A_f , $R_{if,}$ and R_{of} . The basic amplifier configuration without feedback but taking the loading of the β network into account is obtained by applying the following rules:

To find the input circuit:

1. Set $V_o = 0$ for voltage sampling. In other words, short the output node.
2. Set $I_o = 0$ for current sampling. In other words, open the output loop.

To find the output circuit:

1. Set $V_i = 0$ for shunt comparison. In other words, short the input node.
2. Set $I_i = 0$ for series comparison. In other words, open the input loop.

These procedures ensure that the feedback is reduced to zero without altering the loading on the basic amplifier.

Table 5.2 Analysis of feedback amplifiers**.**

S.No.	Type of feedback / Attribute	Voltage-series	Current-series	Current-shunt	Voltage-shunt
1.	Feedback signal	Voltage	Voltage	Current	Current
2.	Sampled signal	Voltage	Current	Current	voltage
3.	To find input loop set	V_o=0	V_o=0	I_o=0	I_o=0
4.	To find output loop set	V_o=0	I_o=0	I_o=0	V_o=0
5.	Signal source	Thevenin's	Thevenin's	Norton's	Norton's
6.	Feedback factor, β	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
7.	Gain, A	$A_V = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
8.	DesensitivityD	$1+\beta A_V$	$1+\beta G_M$	$1+\beta A_I$	$1+\beta R_M$
9.	Gain with feedback, A_f	A_V / D	G_M / D	A_I / D	R_M / D
10.	R_{if}	$R_i D$	$R_i D$	R_i / D	R_i / D
11.	R_{of}	$R_o / (1+\beta A_v)$	$R_o(1+\beta G_m)$	$R_o(1+\beta A_i)$	$R_o / (1+\beta R_m)$
12.	$R'_{of} = R_{of} \mid\mid R_L$	R'_o / D	$R'_o(1+\beta G_m) / D$	$R'_o(1+\beta A_i) / D$	R'_o / D

Th

e complete analysis of a feedback amplifier is obtained by carrying out the following steps:

1. Identity the topology. (a) Is the feedback signal X_f a voltage or a current? In other words, is X_f applied in series or in shunt with the external excitation? (b) Is the samples signal X_o a voltage or a current? In other words, is the sampled signal taken at the output node or from the output loop?
2. Draw the basic amplifier circuit without feedback, following the rules listed above.
3. Use a Thevenin's source if X_f is a voltage and a Norton's source of X_f is a current.
4. Replace each active device by the proper model (for example, the hybrid–π model for a transistor at high frequencies or the *h* – parameter model at low frequencies).
5. Indicate X_f and X_o on the circuit obtained by carrying out steps 2,3 and 4. Evaluate β , using $\beta = X_f / X_o$
6. Evaluate *A* by applying KVL and KCL to the equivalent circuit obtained after step 4.
7. From *A* and β, find *D*, A_f , R_{if} , R_{of} and R'_{of} .

The Stability Problem:

Transfer function of feedback amplifier

$$A_f(s) = \frac{A(s)}{1 + A(s)\beta(s)}$$

For physical frequencies $s = j\omega$, Eq. (10.81) becomes

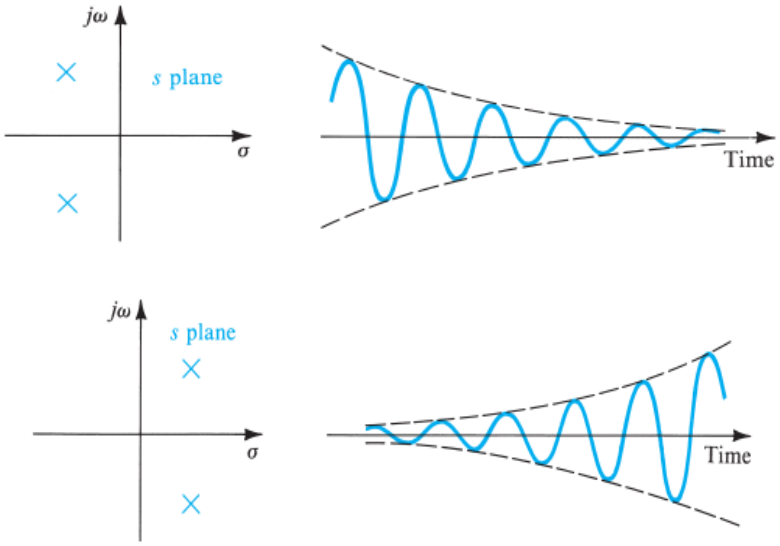
$$A_f(j\omega) = \frac{A(j\omega)}{1 + A(j\omega)\beta(j\omega)}$$

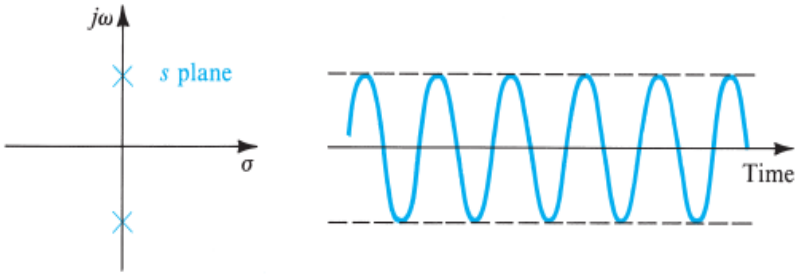
Thus the loop gain $A(j\omega)\beta(j\omega)$ is a complex number that can be represented by its magnitude and phase,

$$L(j\omega) \equiv A(j\omega)\beta(j\omega)$$
$$= |A(j\omega)\beta(j\omega)|e^{j\phi(\omega)}$$

Effect of Feedback on the amplifier poles :

Stability and poles location





Poles of the feedback amplifier :

From the closed-loop transfer function we see that the poles of the feedback amplifier are the zeros of $1 + A(s)\beta(s)$. That is, the feedback-amplifier poles are obtained by solving the equation

$$1 + A(s)\beta(s) = 0$$

which is called the **characteristic equation** of the feedback loop. It should therefore be apparent that applying feedback to an amplifier changes its poles.

Amplifier with single pole response

Consider first the case of an amplifier whose open-loop transfer function is characterized by a single pole:

$$A(s) = \frac{A_0}{1 + s/\omega_P} \tag{10.86}$$

The closed-loop transfer function is given by

$$A_f(s) = \frac{A_0/(1 + A_0\beta)}{1 + s/\omega_P(1 + A_0\beta)}$$

Thus the feedback moves the pole along the negative real axis to a frequency ω_{Pf},

$$\omega_{Pf} = \omega_P(1 + A_0\beta)$$

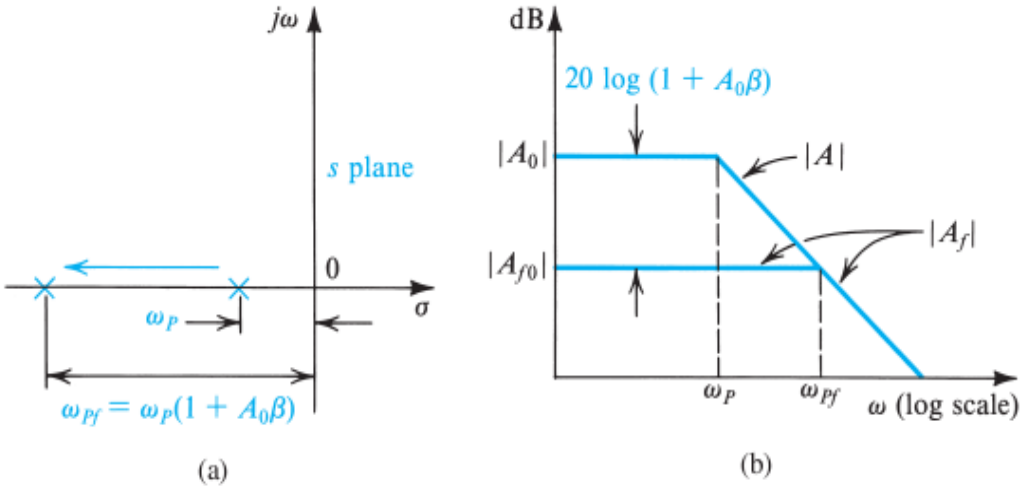


Figure 10.36 Effect of feedback on **(a)** the pole location and **(b)** the frequency response of an amplifier having a single-pole, open-loop response.

Stability study using bode plots :

Gain and phase margins

whether a feedback amplifier is or is not stable can be determined by examining its loop gain Aβas a function of frequency. One of the simplest and most effective means for doing this is through the use of a Bode plot for Aβ.

The difference between the value of at ω180 and unity, called the gain margin, is usually expressed in decibels. The gain margin represents the amount by which the loop gain can be increased while stability is maintained.

Feedback amplifiers are usually designed to have sufficient gain margin to allow for the inevitable changes in loop gain with temperature, time, and so on.

OSCILLATORS

In the design of electronic systems, the need frequently arises for signals having prescribed standard waveforms (e.g., sinusoidal, square, triangle, pulse, etc). These waveforms are commonly used in computers, control systems, communication systems and test measurement systems.

There are two common ways for generating sinusoids:

1. Positive feedback loop with non-linear gain limiting
2. Appropriately shaping other waveforms such as a triangle waves.

SINUSOIDAL OSCILLATORS:

Commonly referred to as linear sine-wave oscillators although some forms of non-linearity have to be employed to limit the output amplitude. Analysis of the circuits is more difficult as s-plane analysis cannot be directly applied to the non-linear part of the circuit. The basic structure of a sinusoidal oscillator consists of an amplifier and a frequency selective network connected in a positive feedback loop.

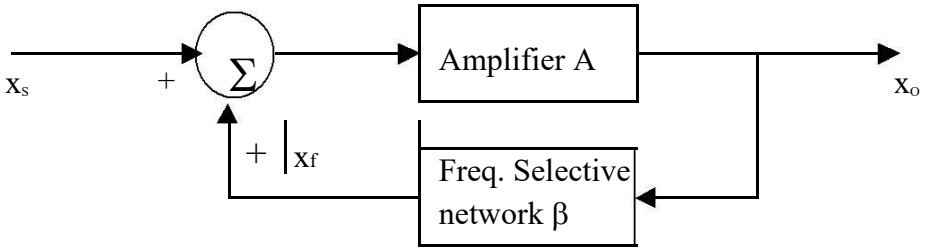


Figure 1: Basic structure of a sinusoidal oscillator.

A positive-feedback loop is formed by an amplifier and a frequency-selective network. In an actual oscillator circuit, no input signal will be present; here an input signal x_s is employed to help explain the principle of operation. Note that the feedback signal X_F is summed with a positive sign:

$$A_f(s) = \frac{A(s)}{1 - A(s)\beta(s)}$$

The loop gain is:

$$L(s) = A(s)\beta(s)$$

And the characteristic equation can be written as:

$$1 - L(s) = 0$$

If at a specific frequency f_0, the loop gain $A\beta$ is equal to unity, it follows that A_f will be infinite. Such a circuit is by definition an oscillator.

Thus for the sinusoidal oscillator at ω_0:

$$L(j\omega 0) = A(j\omega 0) \cdot \beta(j\omega 0) = 1$$

This condition is called Barkhausen Criteria for oscillation, in which:

"UNITY GAIN, ZERO PHASE SHIFT"

It should be noted that the frequency of oscillation ω_0 is determined by the phase characteristics of the feedback loop. The loop oscillates at the frequency for which the phase is ZERO. The steeper the phase shift as a function of frequency $\phi(\omega)$, the more stable the frequency of oscillation.

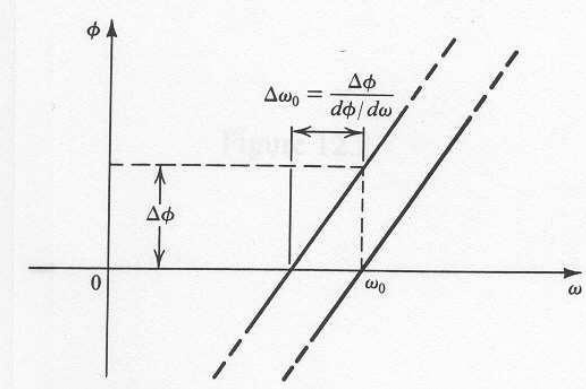


Fig. 12.2 Dependence of the oscillator frequency stability on the slope of the phase response. A steep phase response (that is, large $d\phi/d\omega$) results in a small $\Delta\omega_0$ for a given change in phase $\Delta\phi$ (resulting from a change in a circuit component).

NON-LINEAR AMPLITUDE CONTROL:

Generally, it is difficult to design circuits with $A\beta=1$ as circuit parameters vary with temperature, time, and component values.

If	$A\beta < 1$	oscillator ceases,
If	$A\beta > 1$	oscillation grows until circuit saturates.

It is required to have a mechanism to force $A\beta = 1$. This is accomplished by employing a non-linear circuit for gain control:

- Design circuit with $A\beta > 1$ as voltage of oscillation increases, gain control mechanism kicks in and reduces gain to 1.
- Design circuit with right half plane poles. The gain control pulls the poles back to the imaginary axis.

Two approaches:

1. *The first approach* uses a limiter circuit, oscillations are allowed to grow until the level reaches the limiter set value. Once the limiter comes into operation, the amplitude remains constant. The limiter should be designed to minimize non-linear distortion.
2. *The second method* uses a resistive element in the feedback loop whose resistance can be controlled by the sinusoidal output amplitude. Diodes or JFETs (operating in triode region) are commonly used.

   A popular limiter circuit for amplitude control can be seen below:

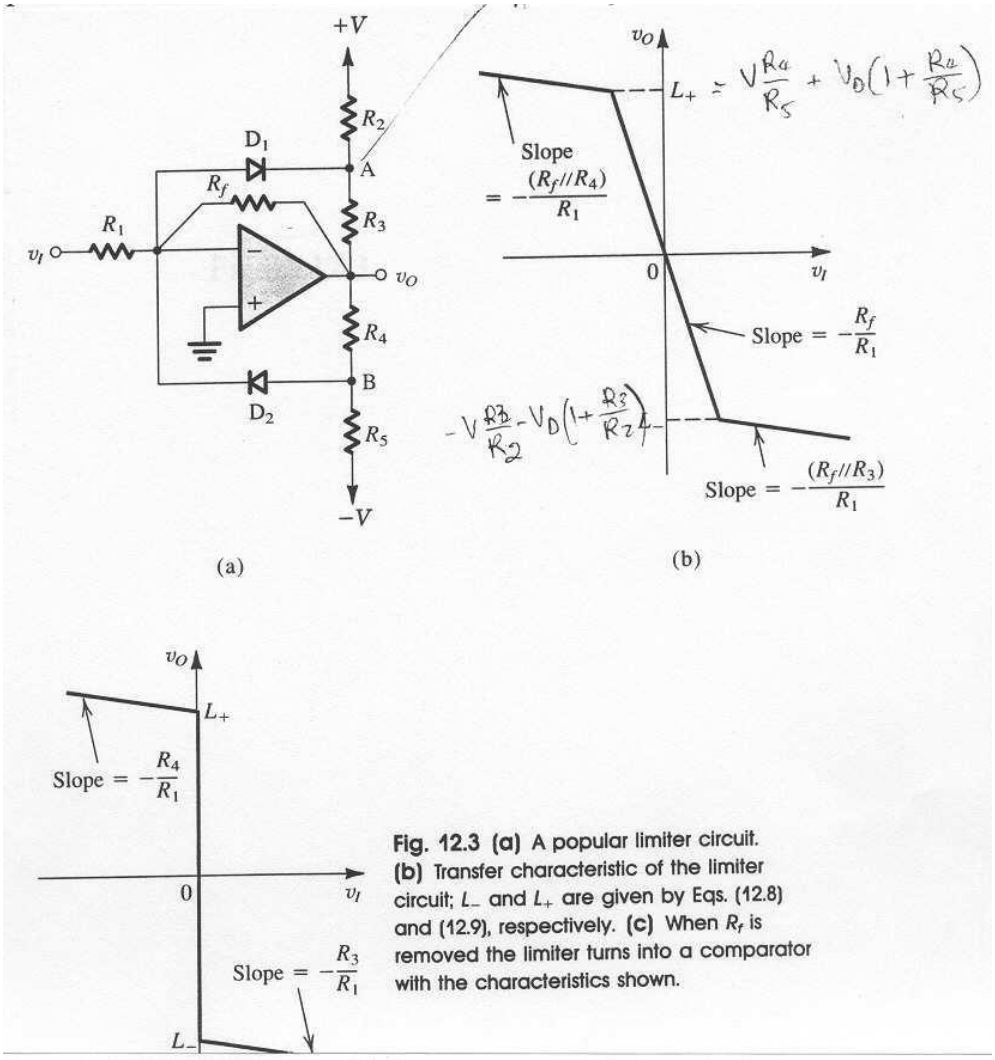
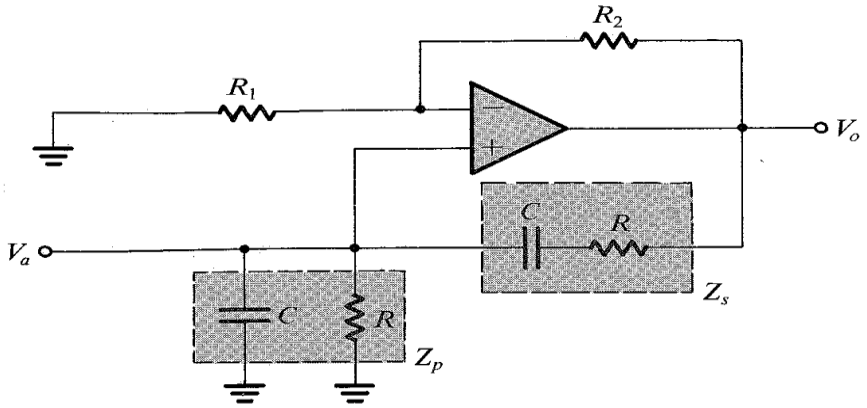


Fig. 12.3 (a) A popular limiter circuit. **(b)** Transfer characteristic of the limiter circuit; L_- and L_+ are given by Eqs. (12.8) and (12.9), respectively. **(c)** When R_f is removed the limiter turns into a comparator with the characteristics shown.

II. OPAMP - RC OSCILLATORS:

1. WIEN-BRIDGE OSCILLATOR



Wien Bridge oscillator without amplitude stabilization

The loop gain can be found by multiplying the transfer function of the feedback path, $V_a(s)/V_0(s)$, by the amplifier gain.

$$L(s) = [1 + \frac{R_2}{R_1}] \quad \frac{Z_P}{Z_P + Z_S}$$

$$L(j\omega) = \frac{1 + \frac{R_1}{R_2}}{3 + j(\omega RC - \frac{1}{\omega RC})}$$

The loop gain will be a real number (i.e., the phase will be zero) at one frequency ω_0 given by:

$$\omega_0 RC = \frac{1}{\omega_0 RC}$$

$$\omega_0 = \frac{1}{RC}$$

To obtain sustained oscillation at this frequency, the magnitude of the loop gain should be unity which can be achieved by setting:

$$\frac{R_2}{R_1} = 2$$

To ensure that oscillation starts, one chooses R2/R1 slightly greater than 2.

The amplitude of the oscillation can be controlled using a non-linear limiter as seen below.

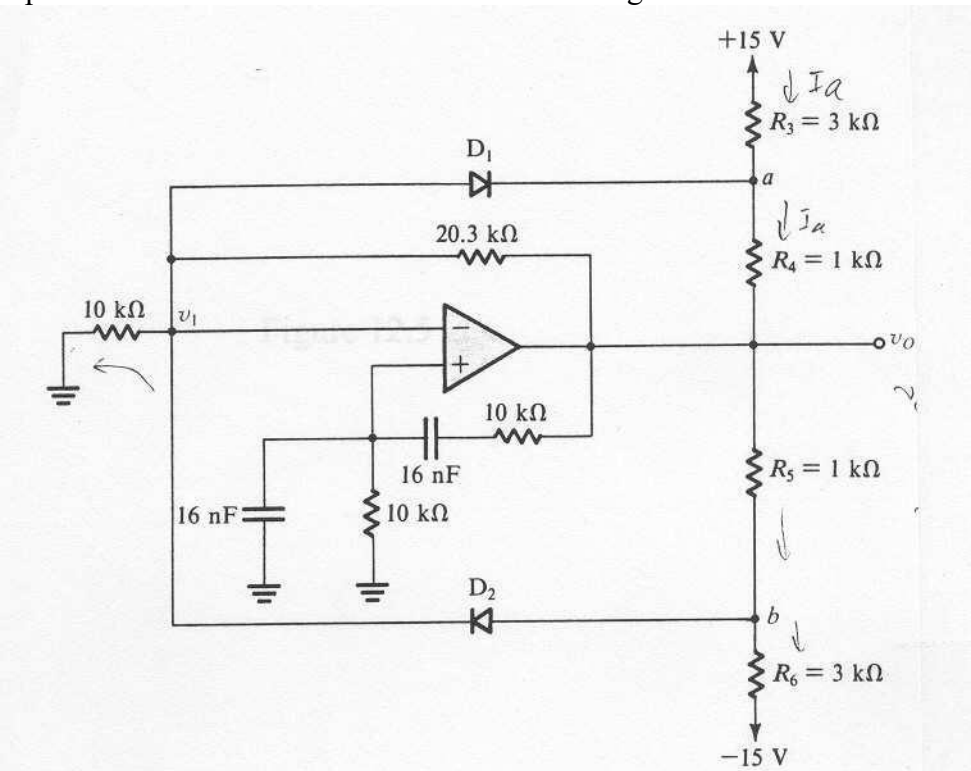


Fig. 12.5 A Wien-bridge oscillator with a limiter used for amplitude control.

2. **PHASE SHIFT OSCILLATOR**

Figure 12.7 shows the basic structure of the phase shift oscillator. It consists of a negative gain amplifier (-K) with a three-section (3rd order) RC ladder network in the feedback.

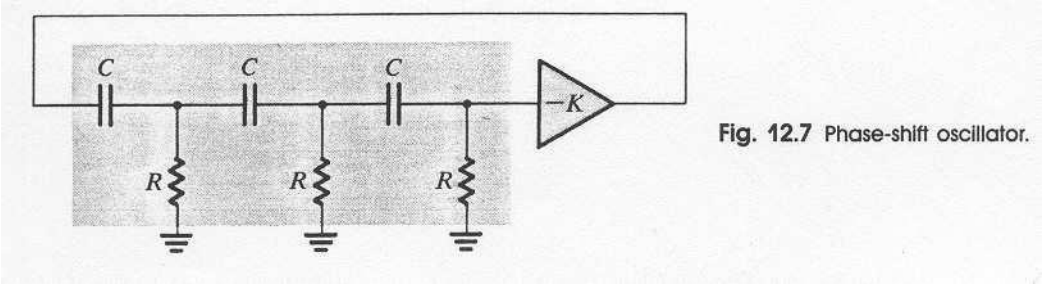


Fig. 12.7 Phase-shift oscillator.

The circuit will oscillate at the frequency for which the phase shift of the RC network is 180^O. **Only at this frequency will the phase shift around the loop be 0^O (360^O)**. Three RC sections are required to produce a 180^O phase shift at a finite frequency.

The value of K is chosen to be slightly higher than the inverse of the magnitude of the RC network transfer function at the frequency of oscillation.

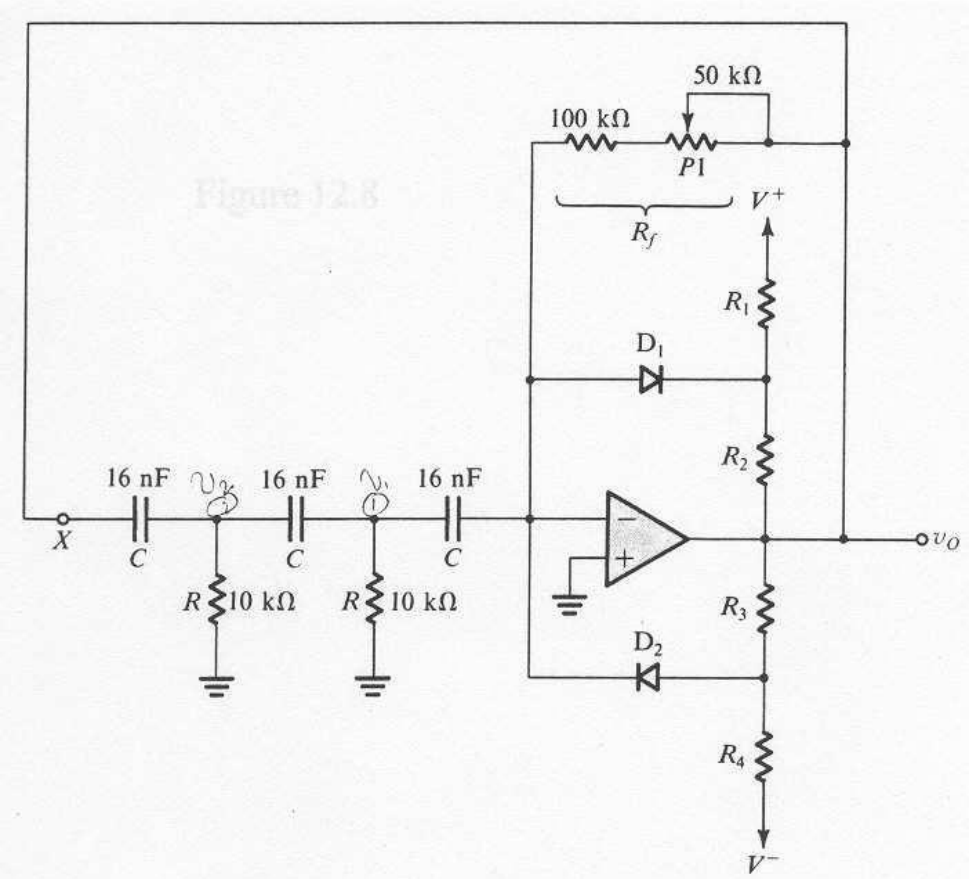


Fig. 12.8 Practical phase-shift oscillator with a limiter for amplitude stabilization.

3. ACTIVE FILTER TUNED OSCILLATOR

In this type of filter, Figure 12-10, a filter is used to select a particular frequency in the spectrum of a square wave (usually the fundamental frequency). Output of the filter is a sinewave and is taken as the output of the oscillator. The output is fed back to a limiter which is used to convert a sinewave to a squarewave. The squarewave signal then becomes the input of the filter.

The actual circuit is shown in Figure 10.11, the limiter is a pair of diodes to have a squarewave at v2. This filter is an active filter (we will study this filter later) to select the fundamental frequency and provides the output at v1.

The op-amp RC oscillator circuits are useful for operation in the 10Hz-1MHz range due to limitations in passive component size (low frequency) and op-amp slew rate (high frequency). For higher frequencies, circuits that employ transistors together with LC tuned circuits or crystals are commonly used.

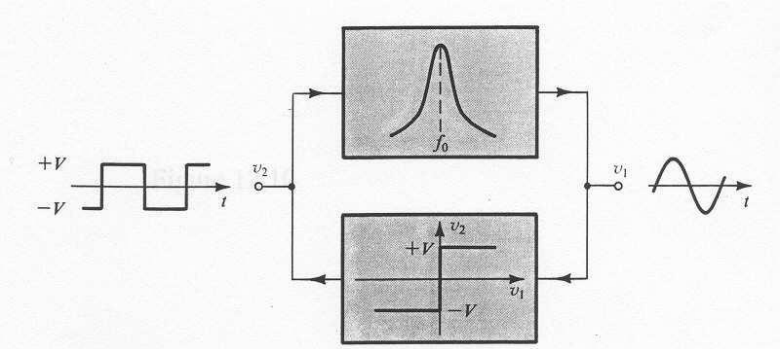


Fig. 12.10 Block diagram of the active-filter tuned oscillator.

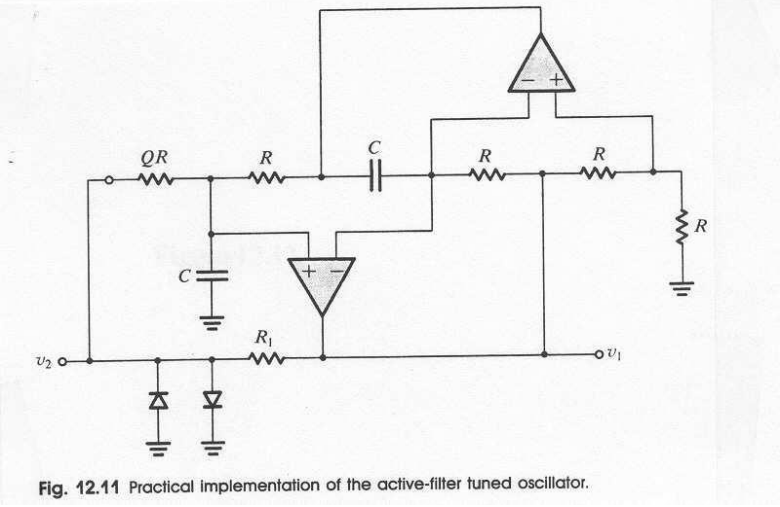


Fig. 12.11 Practical implementation of the active-filter tuned oscillator.

III. LC AND CRYSTAL OSCILLATORS:

Oscillators utilizing transistors and LC tuned circuits or crystals are useful for operation in the range from 100KHz to 500MHz. They exhibit higher Q than RC types (more stable). However, LC oscillators are difficult to tune over wide range of frequency and crystal oscillator operates at a single frequency. The extremely stable response of the crystal oscillators has made them very popular, particularly for digital timing signals.

LC TUNED OSCILLATOR

Two common used configurations are the Colpitts and the Hartley oscillators. The basic circuit structures without biasing can be seen below.

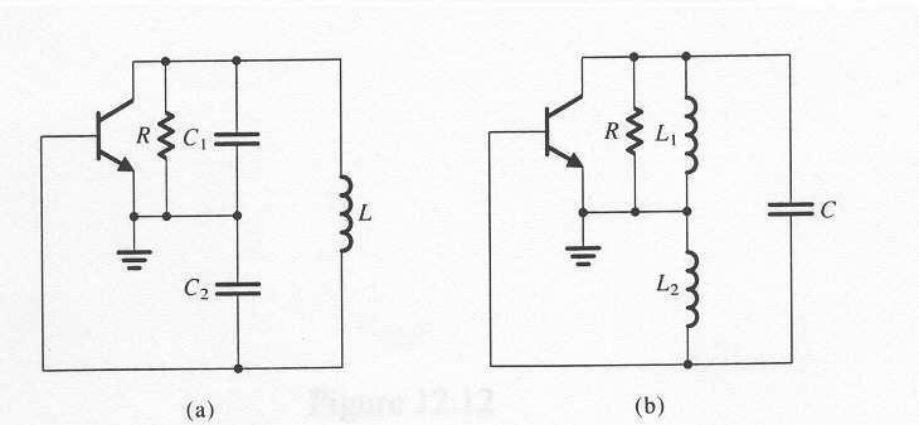


Fig. 12.12 Two commonly used configurations of LC-tuned oscillators: **(a)** Colpitts; **(b)** Hartley.

Both circuits utilize a parallel LC circuit connected between the collector and the base with a fraction of the tuned circuit voltage fed to the emitter of the transistor. The resistor R models the losses of the inductor, the load resistance of the oscillator and the output resistance of the transistor.

If the frequency of operation is sufficiently low, we can neglect the transistor parasitic capacitances. The frequency of oscillation is determined by the resonant frequency of the parallel tuned circuit (also known as a tank circuit). For the Colpitts oscillator:

$$\omega 0 = \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

For the Hartley oscillator

$$\omega 0 = \frac{1}{\sqrt{C(L_1 + L_2)}}$$

The ratio L_1/L_2 or C_1/C_2 determines the feedback factor and thus must be adjusted in conjunction with the transistor gain to ensure that oscillations will start.

To determine the oscillation condition for the Colpitts oscillator, we replace the transistor with its equivalent circuit. To simplify the analysis, we neglect the transistor capacitances except capacitance C_{BE} is a part of C2.

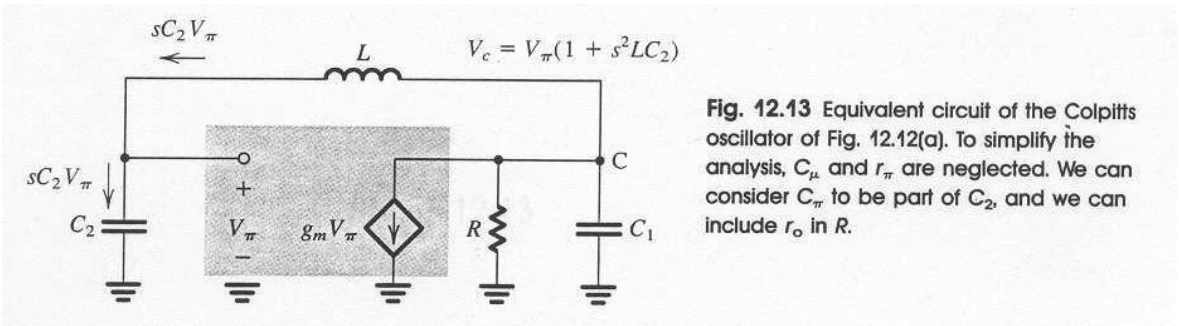


Fig. 12.13 Equivalent circuit of the Colpitts oscillator of Fig. 12.12(a). To simplify the analysis, C_μ and r_π are neglected. We can consider C_π to be part of C_2, and we can include r_o in R.

A node equation at the transistor collector (C) yields:

$$sC_2 V_\pi + g_m V_\pi + \left(\frac{1}{R} + sC_1\right)\left(1 + s^2 LC_2\right)V_\pi = 0$$

Since $V_\pi \neq 0$ (oscillations have started), it can be eliminated (i.e., the other terms are zero).

$$s^3 LC_1C_2 + s^2\left(L\frac{C}{R^2}\right) + s(C_1 + C_2) + \left(\overline{gm} + R^1\right) = 0$$

$$\left(g_m + \frac{1}{R} - \frac{\omega^2 LC_2}{R}\right) + j[\omega(C_1 + C_2) - \omega^3 LC_1C_2] = 0$$

For oscillations to start, both the real and imaginary parts must be zero.

Setting the imaginary part to zero gives

$$\omega 0 = \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

which is the resonant frequency of the tank circuit.

Setting the real part to zero yields

$$\frac{C2}{C1} = gmR$$

For sustained oscillation, the magnitude of the gain from the base to collector (g_mR) must be equal to the inverse of the voltage ratio provided by the capacitive divider:

$$\frac{V_{be}}{V_{ce}} = \frac{C_1}{C2}$$

For oscillation to start, the loop gain must be greater than unity which is equivalent to

$$gmR > \frac{C_2}{C1}$$

As oscillation grows in amplitude, the transistors non-linear characteristics reduce the loop gain to unity, thus sustaining oscillations. An example of a complete Colpitts oscillator is shown below

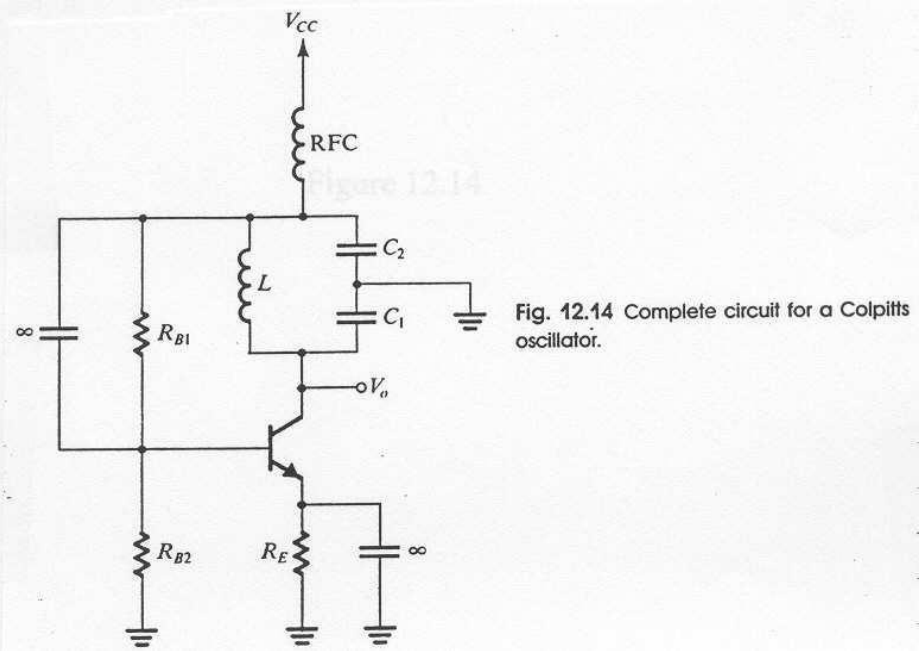


Fig. 12.14 Complete circuit for a Colpitts oscillator.

The radio frequency choke (RFC) in this oscillator provides a high reactance at ω_0 but a low DC resistance. Unlike the op-amp oscillators that incorporate special amplitude control circuitry, LC tuned oscillators utilize the non-linear i_c-v_{be} characteristics of the BJT (or i_d versus v_{gs} for FET) for amplitude control. As the oscillations grow, the effective gain of the transistor is reduced below its small signal value. The LC tuned oscillators are known as self-limiting oscillators.

Reliance on the non-linear characteristics of the BJT (or the FET) implies that the collector (drain) current waveform will be nonlinearity distorted. Nevertheless, sinusoidal of high purity because of the filtering action of the LC tuned circuit.

CRYSTAL OSCILLATORS

A piezoelectric crystal, such as quartz, exhibits electro-mechanical resonant characteristics that are very stable (with time and temperature) and high selectivity (having very high Q factor). The circuit symbol of a crystal is shown below.

The resonant properties are characterized by a large inductance L (as high as hundreds of Henrys), a very small series capacitance C_s (as small as 0.0005pF), a series resistance r representing a Q factor ($Q=\omega_0 L/r$ that can be as high as few hundred thousand) and a parallel capacitance C_p (a few picoFarad).

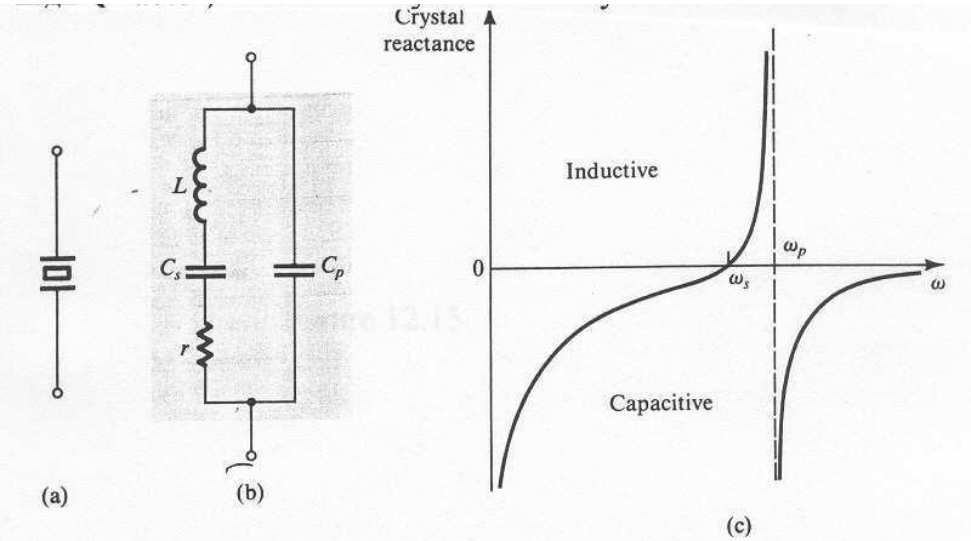


Fig. 12.15 A piezoelectric crystal: **(a)** circuit symbol; **(b)** equivalent circuit; **(c)** crystal reactance versus frequency [note that, neglecting the small resistance r, $Z_{crystal} = jX(\omega)$].

Capacitance C_p represents the electrostatic capacitance between the two parallel plates of the crystal ($C_p >> C_s$). Since the Q factor is so high, we can neglect the resistance r and express the crystal impedance as:

$$Z(s) = \frac{1}{sC_p + \dfrac{1}{sL + 1/sC_s}}$$

which can be manipulated to the form

$$Z(s) = \frac{1}{sC_p} \frac{s^2 + \dfrac{1}{LC_s}}{s^2 + \dfrac{C_p + C_s}{L(C_pC_s)}}$$

we see that the crystal has two resonant frequencies:

$$\omega_s = \frac{1}{\sqrt{LC_s}} \quad \text{and} \quad \omega_p = \frac{1}{\sqrt{\dfrac{C_sC_p}{LC_s + C_p}}}$$

they are **series resonance and parallel resonance**.

For $s = j\omega$

$$Z(j\omega) = -j \frac{1}{\omega C_p} \left(\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2} \right)$$

It can be seen that $\omega_p > \omega_s$, however, since $C_p >> C_s$, the two resonant frequencies are very close.

From Figure 12.15, we observe that the crystal reactance is inductive over a narrow frequency band between ω_p and ω_s. We may use the crystal to replace the inductor in a Colpitts oscillator. The resulting circuit will oscillate at the resonant frequency of the crystal inductance L with the series equivalent of C_s and $(C_p + \frac{C1C2}{C1 + C2})$.

Since C_s is much smaller than the other capacitances, it will dominate and

$$\omega_0 = \frac{1}{\sqrt{LC_S}} = \omega_s$$

A popular configuration of the Colpitts oscillator called Pierce oscillator is shown below.

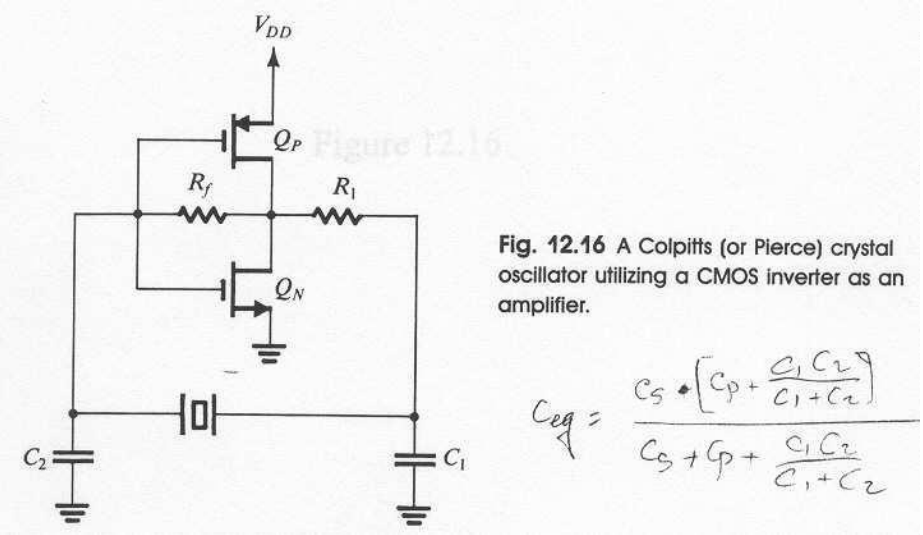


Fig. 12.16 A Colpitts (or Pierce) crystal oscillator utilizing a CMOS inverter as an amplifier.

$$C_{eq} = \frac{C_S \cdot \left[C_p + \frac{C_1 C_2}{C_1 + C_2}\right]}{C_S + C_p + \frac{C_1 C_2}{C_1 + C_2}}$$

Resistor Rf determines the DC operating point in the high gain region of the CMOS inverter. Resistor R1 together with capacitor C1 provides a LPF that discourages the circuit from oscillating at higher harmonic of the crystal frequency.

Common to purchase crystal modules with TTL, CMOS or ECL outputs with 14 pin dip or surface mount. Crystals are available in standard frequencies and can be custom ordered for relatively low cost. The oscillators can be tuned a small amount with the use of variable capacitor (varactor) to create Voltage Control Crystal Oscillator (VCXO). Crystals are also be used in high Q filters such as crystal filters or SAW filters.

ANALOG CIRCUITS UNIT-V

ASSIGNMENT CUM TUTORIAL QUESTIONS

A. Questions testing his remembering / understanding level of students

I. Objective/ Multiple Choice Questions

1. When negative voltage feedback is applied to an amplifier, its voltage gain is [ ]

a) Decreases b) increases c) remains the same d) none of the above

2. The value of negative feedback fraction is always [ ]

a) Less than 1 b) Greater than 1 c) equal to 1 d) none of the above

3. If the feedback fraction of an amplifier is 0.01, then voltage gain with negative Feedback is approximately ……. [ ]

a) 10 b) 100 c) 1000 d) 0.01

4. The gain of an amplifier with feedback is known as …….. gain [ ]

b) Open loop gain b) closed loop gain c) Resonant d) none of the above

5. Negative feedback is employed in …….. [ ]

a) Oscillators b) Amplifiers c) Rectifiers d) None of the above

6. When a negative voltage feedback is applied to an amplifier, its bandwidth…….[ ]

a) Decreases b) increases c) remains the same d) none of the above

7. List some advantages of negative feedback amplifiers.

8. Gain increases with positive feedback [Y/N]

9. What would be the computational value of feedback voltage in a negative feedback Amplifier with$A = 100$, $\beta = 0.03$ and input signal voltage = 30 mV [ ]

a) 0.03 b) 0.06 c) 0.09 d) 0.15

10. Define Desensitivity

II) Descriptive Questions

1.List the advantages of Negative Feedback and also draw the general structure of Feedback amplifiers with negative Feedback.

2.List the basic feedback topologies.

3.Whatis the type of feedback topology used in Voltage amplifier?. Draw its basic structure.

4.What is the type of feedback topology used in Current amplifier? Draw its basic structure.

5.What is the type of feedback topology used in Trans Conductance amplifier? Draw its basic structure.

6.What is the type of feedback topology used in Trans Resistance amplifier? Draw its basic structure.

7.What is Gain Margin & Phase Margin? How they are for a stable Amplifier.

8. Draw the feedback structure and derive the expression for feedback gain with Negative Feedback.

9. Explain how the Negative feedback improve Gain Desensitization, and Bandwidth extension.

11. Derive expressions for input and output resistances of a series-shunt feedback amplifier.

12. Derive expressions for input and output resistances of a Shunt-Series feedback amplifier

13. Derive expressions for input and output resistances of a Series-Series feedback amplifier.

14. Derive expressions for input and output resistances of a series-shunt feedback amplifier.

Explain the effect of Feedback on Amplifier with Single- Pole response.

Derive expressions for input and output resistances of a Shunt-Shunt feedback amplifier

B. Question testing the ability of students in applying the concepts.

I) Multiple Choice Questions:

1. Emitter follower is a …….. circuit [ ]

a) Voltage feedback b) Current feedback c) Current &Voltage feedback d) none of the above

2. If voltage feedback (negative) is applied to an amplifier, its output impedance …….. [ ]

a) Increases b) decreases c) remains same d) none of the above

3. For voltage amplifiers [ ]

a) $R_i$increases, R_o increases b) $R_i$increases, R_o decreasesc)$R_i$decreases, R_o increasesd)$R_i$decreases, R_o decreases

4. For Current amplifiers [ ]

a) $R_i$increases, R_o increases b) $R_i$increases, R_o decreasesc)$R_i$decreases, R_o increases d)$R_i$decreases , R_o decreases

5. For Trans conductance amplifiers [ ]

a) $R_i$increases, R_o increases b) $R_i$increases, R_o decreasesc)$R_i$decreases, R_o increases d)$R_i$decreases, R_o decreases

6. For Trans resistance amplifiers [ ]

a) $R_i$increases, R_o increases b) $R_i$increases, R_o decreasesc)$R_i$decreases, R_o increases d)$R_i$decreases, R_o decreases

7. Which type of amplifier is a voltage controlled voltage source [ ]

a) voltage amplifiers b) Current amplifiers c) Trans conductance d) Trans resistance

8. Which type of amplifier is a voltage controlled voltage source [ ]

a) voltage amplifiers b) Current amplifiers c) Trans conductance d) Trans resistance

9. Which type of amplifier is a voltage controlled voltage source [ ]

a) voltage amplifiers b) current amplifiers c) Trans conductance d) Trans resistance

10. Which type of amplifier is a voltage controlled voltage source [ ]

a) voltage amplifiers b) current amplifiers c) Trans conductance d) Trans resistance

II. PROBLEMS

1.) Explain how the application of Negative feedback reduces Interference and Non-linear Distortion. b) A feedback amplifier has a Forward Gain of A = 1000 & β = 0.001. Find the amount of feedback, Closed loop Gain Af .

2. A series-shunt feedback amplifier employs a basic amplifier with input and output resistance of 1kΩ each and gain A=2000. If feedback factor β=0.1, find Af, Rif, Rof of closed loop amplifier.

3. A Shunt-Series feedback amplifier employs a basic amplifier with input and output resistance of 1kΩ each and gain A=1000. If feedback factor β=0.002, find Af, Rif, Rof of closed loop amplifier.

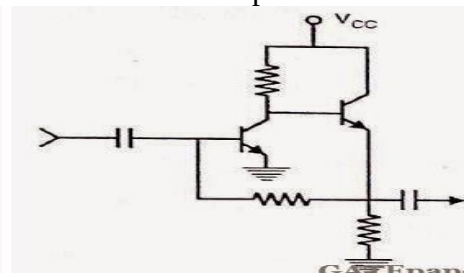
4. A series-series feedback amplifier employs a basic amplifier with input and output resistance of 15kΩ each and gain A=2000. If feedback factor β=0.1, find Af, Rif, Rof of closed loop amplifier.

5. A series-shunt feedback amplifier employs a basic amplifier with input and output resistance of 10kΩ each and gain A=2000. If feedback factor β=0.01, find Af, Rif, Rof of closed loop amplifier.

6. An op amp having a single-pole roll off at 5000 Hz and a low-frequency gain of 200 is operated in a feedback loop with β =0.01. What is the factor by which Feedback Shifts pole? To What Frequency?
7. A feedback amplifier has a Forward Gain of A = 2000& β = 0.01. Find a) Closed loop Gain Af, b) Amount of Feedback & c) If A decreases by 10% what is the corresponding decrease in Af .

D.Previous GATE/ IES Questions

1. The feedback amplifier shown in figure has [ ]**{2000}**



a) Current series feedback with large input impedance and large output impedance
b) Voltage series feedback with large input impedance and large output impedance
c) Voltage shunt feedback with large input impedance and large output impedance
d) Current shunt feedback with large input impedance and large output impedance

2. Negative feedback in amplifiers [ ] **{2004}**
a) Improves signal to noise ratio at the input
b) Improves signal to noise ratio at the output
c) Reduces distortion
d) Does not affect the signal to noise ratio at the output

3. To obtain high input, output impedances …….type of feedback topology is used [ ] **{2002}**
a) Voltage series b) voltage shunt c) current series d) current shunt

4. Negative feedback amplifier is an amplifier [ ] **{2009}**
a) Reduces gain b) reduces bandwidth c) increases noise d) increases frequency and phase distortions

5. In a shunt negative type of feedback amplifiers [ ] **{2011}**
a) High input impedance and high output impedance
b) high input impedance and low output impedance
c) low input impedance and low output impedance
d) low input impedance and high output impedance

A. Questions testing his remembering / understanding level of students

I. Objective/ Multiple Choice Questions

1. Only the condition A β = _____ must be satisfied for self-sustained [ ]

Oscillations to result.

A) 0 B) 1 C) -1 D) none of the above

2. Sinusoidal oscillators operate with _____ feedback.

3. Which of the following is required for oscillation? [ ]

A) A $\beta > 1$

B) The phase shift around the feedback network must be 180^o.

C) Both A $\beta > 1$ and the phase shift around the feedback network must be 180^o.

D) None of the above

4. In order to start up, a feedback oscillator requires [ ]

A) Negative feedback less than 1

B) Positive feedback greater than 1

C) Unity feedback equal to 1

D) No feedback

5. Which of the following oscillators is (are) tuned oscillators? [ ]

A) Colpitts B) Hartley C) Crystal D) All of the above

6. One condition for positive feedback is that the phase shift around the feedback loop must be ----------.degrees.

7. An input signal is needed for an oscillator to start [T/F]

8. At series resonance, the impedance of a crystal is [ ]

A) Minimum B) Maximum C) zero D) one

9. Define an Oscillator.

10. At Parallel resonance, the impedance of a crystal is [ ]

A) Minimum B) Maximum C) zero D) one

11. Which of the following is an audio oscillator? [ ]

A) Wein bridge B) Hartley C) Collpits D) Crystal

II) Descriptive Questions

1) Explain about the Barkhausen Criterion and also detail the dependency of oscillator frequency on slope of the phase response.
2) Explain about the Non linear Amplitude control.

3) Derive the expression for frequency of oscillations and the condition for starting oscillations of a wein-bridge oscillator.
4) Explain the operation of RC Phase shift oscillator and derive the expression for frequency of oscillations.
5) Explain the operation of Quadrature oscillator and derive the expression for frequency of oscillations.
6) Derive the expression for frequency of oscillations and the condition for starting oscillations of a Hartley oscillator.
7) Derive the expression for frequency of oscillations and the condition for starting oscillations of Collpits oscillator.
8) Explain in detail about Crystal Oscillator.

B. Question testing the ability of students in applying the concepts.

I) Multiple Choice Questions:

1. **An oscillator converts** …….. [ ]

A. AC power into DC power

B. DC power into AC power

C. Mechanical power into DC power

D. None of the above

2. In Wein bridge oscillator frequency of oscillation is ……. [ ]

A. Inversely proportional to RC

B. Directly proportional to RC

C. Doesn't depends on RC

D. None of the above

3**. In an LC oscillator, if the value of L is increased four times, the frequency of oscillations is ……** [ ]

A. Increased 2 times B. Decreased 2 times

C. Increased 4 times D. Decreased 4 times .

4. In **an wein bridge oscillator, if the value of R is increased four times, the frequency**

of oscillations is …… [ ]

A. Increases B. Decreases C. Remains the same D. Insufficient data

5. **If the crystal frequency increases with temperature, we say that crystal has …….**

temperature coefficient. [ ]

A. Positive B. negative C. zero D. none

6. At series or parallel resonance, the circuit behaves as a …….. load

A. Capacitive B. Resistive C. Inductive D. None of the above

II) Problems:

1) For the popular limiter circuit with V = 15 V, R_1 = 30 kΩ, R_f = 60 kΩ, R_2 = R_5 = 9 kΩ, and R_3 = R_4 = 3kΩ, find the limiting levels and the value of V_I at which the limiting levels are reached. Also determine the limiter gain and the slope of the transfer characteristic in the positive and negative limiting regions. Assume that V_D = 0.7 V.

2.) Consider a sinusoidal oscillator formed of an amplifier with a gain of 2 and a second-order band pass filter. Find the pole frequency and the center-frequency gain of the filter needed to produce sustained oscillations at 1 kHz

3.) For the circuit of Wien-bridge oscillator with a limiter used for amplitude control (a) Disregarding the limiter circuit, find the location of the closed-loop poles. (b) Find the frequency of oscillation. (c) With the limiter in place, find the amplitude of the output sine wave (assume that the diode drop is 0.7 V).

4.) Using a BJT biased at I_C = 1 mA, design a Colpitts oscillator to operate at ω_0 = 106 rad/s. Use C_1 = 0.01 μF and assume that the coil available has a Q of 100 (this can be represented by a resistance in parallel with C_1 given by $Q/\omega_0 C_1$). Also assume that there is a load resistance at the collector of 2 kΩ and that for the BJT, ro = 100 kΩ. Find C_2 and L.

5.) A 2-MHz quartz crystal is specified to have L = 0.52 H, Cs = 0.012 pF, Cp = 4 pF, and r = 120 Ω.. Find fs, fp, and Q.

C. Question testing Analyzing/evaluating/Creative abilities of Student

1. An oscillator is formed by loading a trans conductance amplifier having a positive gain with a parallel RLC circuit and connecting the output directly to the input (thus applying positive feedback with a factor β = 1). Let the trans conductance amplifier have an input resistance of 10 kΩ and an output resistance of 10 kΩ.. The LC resonator has L = 10 μH, C = 1000 pF, and Q = 100. For what value of trans conductance Gm will the circuit oscillate? At what frequency ?

2. For the circuit in Fig.1, find L(s), L(jω), the frequency for zero loop phase, and for oscillation.

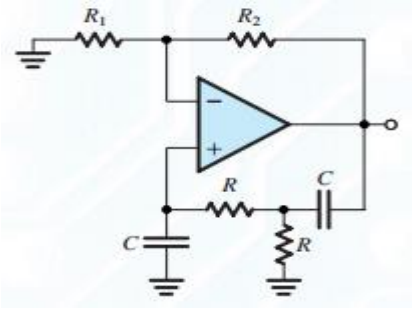


Figure 1

3. For the circuit in Fig.2, find L(s), L(jω), the frequency for zero loop phase, and for oscillation.

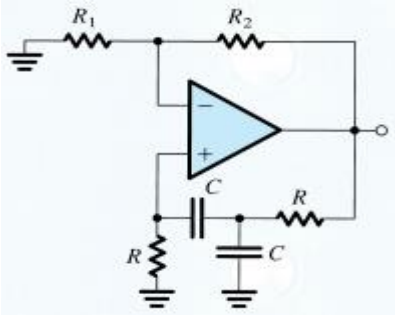


Figure 2

4. For the circuit in Fig.3, break the loop at node X and find the loop gain (working backward for simplicity to find Vx in terms of V_o). For R = 10 kΩ, find C and R_f to obtain sinusoidal oscillations at 10 kHz.

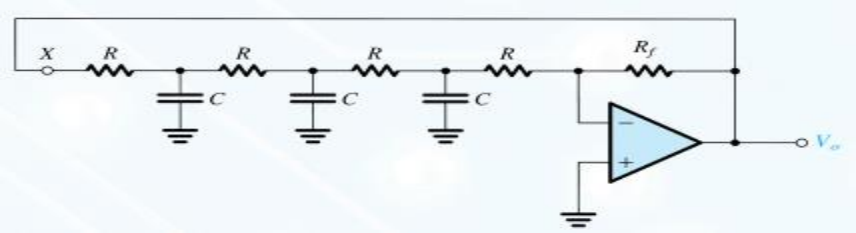


Figure 3

5. Consider the circuit of Fig. 4 without the limiter. Break the feedback loop at X and find the loop gain. To do this, it is easier to start at the output and work backward, finding the various currents and voltages, and eventually V_x in terms of V_o.

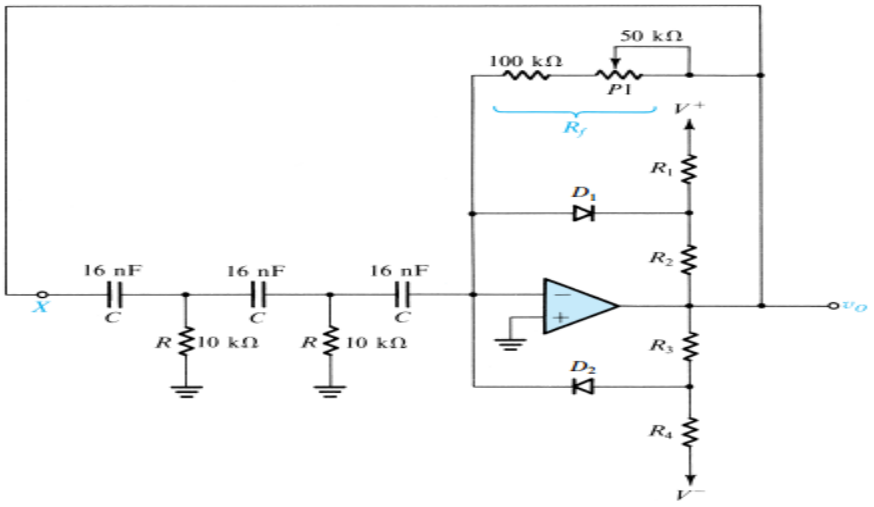
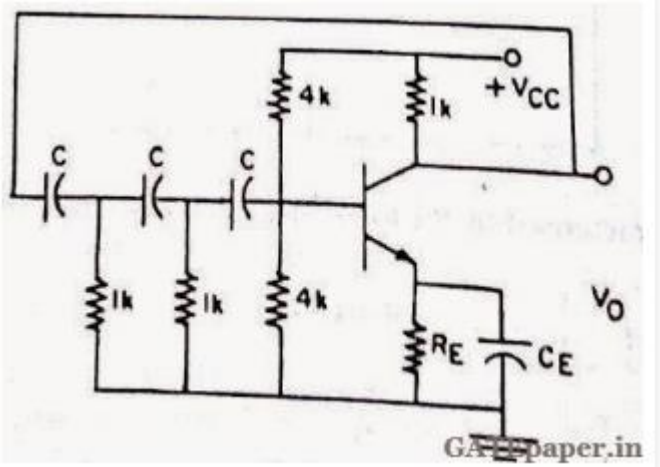


Figure 4

6. Use the expression derived in Q.no 5 to find the frequency of oscillation f_0 and the minimum required value of R_f for oscillations to start in the circuit of Fig. 4.

D. Previous GATE/ IES Questions

1. The below figure shows an RC phase shift oscillator **(GATE 2011)**



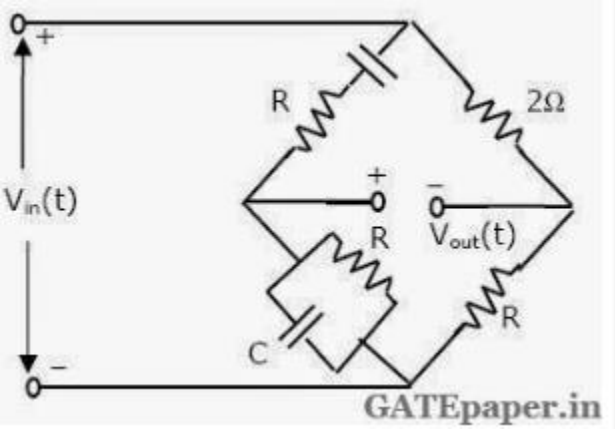
Solve the network and find the possible value of h_{fe} for the transistor for oscillations to be possible. Also determine the frequency of such oscillations. Take C=0.01μF and h_{ie}= 2kΩ.

2. Match the following **(GATE 2012)**

a) Hartley	1) Low frequency Oscillator
b) Collpits	2) High frequency Oscillator
c) Crystal	3) Stable frequency Oscillator

4) Relaxation frequency Oscillator
5) Negative resistance Oscillator

3. Calculate the frequency at which the zero transmission is obtained from the Wein Bridge shown below



In the circuit shown below, capacitors C_1 and C_2 are very large and acts as short at input frequency, V_i is a small signal input, The gain magnitude at 10M rad/s **(GATE 2014)**

UNIT-VI
Output Stages and Power Amplifiers

Introducition:

An important function of the output stage is to provide the amplifier with a low output resistance so that it can deliver the output signal to the load without loss of gain. Since the output stage is the final stage of the amplifier, it usually deals with relatively large signals. Thus the small-signal approximations and models either are not applicable or must be used with care.

The most challenging requirement in the design of an output stage is for it to deliver the required amount of power to the load in an efficient manner. This implies that the power dissipated in the output-stage transistors must be as low as possible.
This requirement comes mainly from the fact that the power dissipated in a transistor raises its internal junction temperature, and there is a maximum temperature (in the range of 150°C to 200°C for silicon devices) above which the transistor is destroyed.

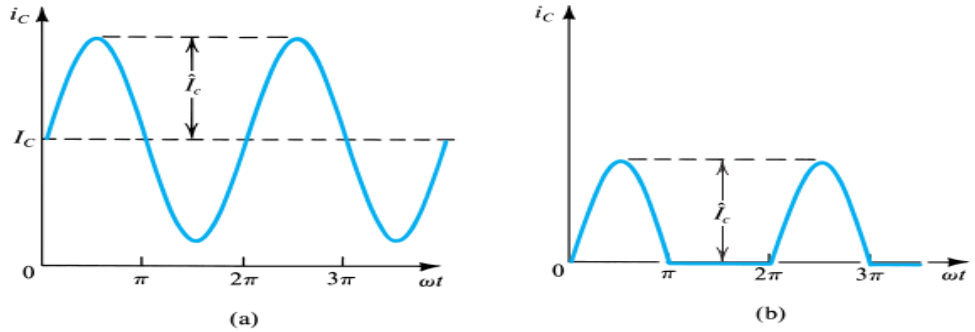
A power amplifier is simply an amplifier with a high-power output stage.

Classification of Output Stages:

Output stages are classified according to the collector current waveform that results when aninput signal is applied.

The transistor in a **class A stage** conducts for the entire cycle of the input signal; that is, the conduction 360° as shown in Fig(a).

The transistor in **class B stage** is biased at zero dc current i.e in cut off. Thus a transistor in a class B stage conducts for only half the cycle of the input sine wave, resulting in a conduction angle of 180° as shown in Fig(b).



An intermediate class between A and B, appropriately named **class AB,** involves biasing the transistor at a nonzero dc current much smaller than the peak current of the sine-wave signal. As a result, the transistor conducts for an interval slightly greater than half a cycle, as illustrated in Fig.(c). The resulting conduction angle is greater than 180°but much less than 360°.

The transistor **in Class C** conducts for an interval shorter than that of a half-cycle; that is, the conduction angle is less than 180° as in Fig (d). The result is the periodically pulsating current waveform shown. To obtain a sinusoidal output voltage, this current is a parallel LC circuit, tuned to the frequency of the input sinusoid.

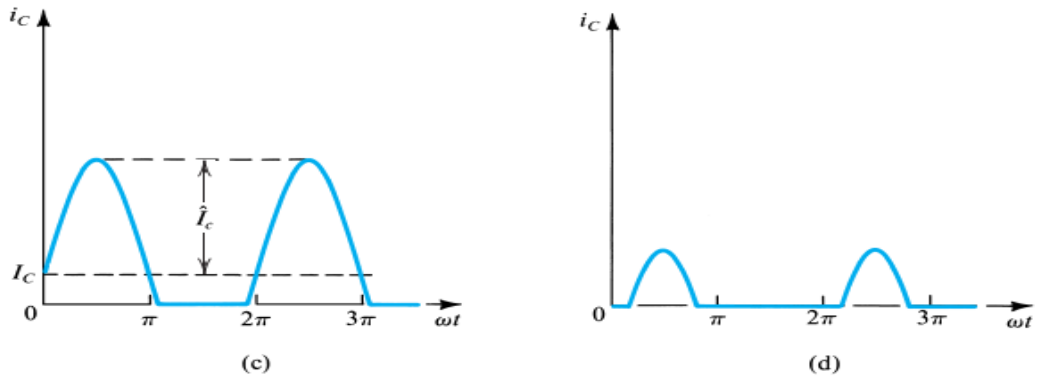


Fig 1. Collector current waveforms for transistors operating in (a)class A, (b)class B, (c)class AB, and (d)class C amplifier stages.

Note: Class A, AB, and B amplifiers are studied in this chapter. They are employed as output stages of op amps and audio power amplifiers. In the latter application, class AB is the pre-ferred choice, for reasons that will be explained in the sections to follow. Class C amplifiers are usually employed for radio-frequency (RF) power amplification (required, e.g., in mobile phones and radio and TV transmitters)

Class A Output Stage:

The most popular class a output stage uses emitter follower because of its low output resistance.

An emitter follower Q1 biased with a constant current I supplied by transistorQ2. Since the emitter current i_{E1}= I + i_L, the bias current I must be greater than the largest negative load current; otherwise, Q1 cuts off and class A operation will no longer be maintained.

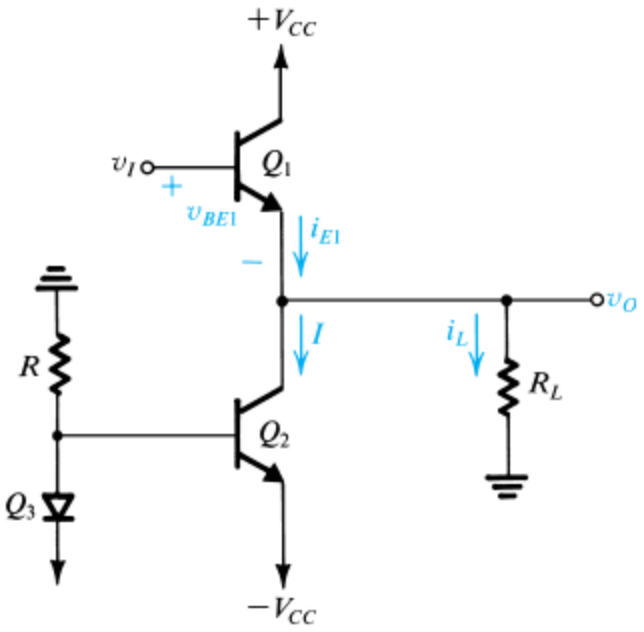


Fig. An emitter follower (Q1)biased with a constant current I supplied by transistor Q2

The transfer characteristic of the emitter follower is described by

$$v_O = v_I - v_{BE1} \quad \text{----------(1)}$$

the linear transfer curve is shown below, the positive limit of the linear region is determined by the saturation of Q1; thus

$$v_{O\max} = V_{CC} - V_{CE1\text{sat}} \quad \text{----------(2)}$$

In the negative direction, depending on the values of I and R_L, the limit of the linear region is determined either by Q1turning off or by Q2saturating,

$$v_{O\min} = -IR_L \quad \text{----------(3)}$$

$$v_{O\min} = -V_{CC} + V_{CE2\text{sat}} \quad \text{----------(4)}$$

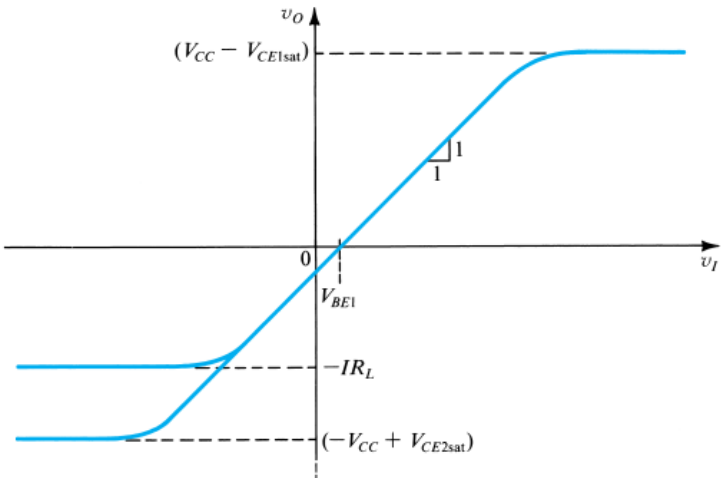


Fig. Transfer characteristic of the emitter follower

The absolutely lowest (most negative) output voltage is that given by Eq. (4) and is achieved provided the bias current I is greater than the magnitude of the corresponding load current

$$I \geq \frac{|-V_{CC} + V_{CE2sat}|}{R_L} \quad \text{---------(5)}$$

Power-Conversion Efficiency:

The power-conversion efficiency of an output stage is defined as

$$\eta \equiv \frac{\text{Load power } (P_L)}{\text{Supply power } (P_S)} \quad \text{.....(6)}$$

For the Claas- A using emitter follower assuming that the output voltage is a sinusoid with the peak value , $\hat{V}_o$, the average load power will be

$$P_L = \frac{(\hat{V}_o/\sqrt{2})^2}{R_L} = \frac{1}{2}\frac{\hat{V}_o^2}{R_L} \quad \text{....(7)}$$

Since the current in Q2 is constant (I), the power drawn from the negative supply is V_{CC} * I. The average current in Q1 is equal to I, and thus the average power drawn from the positive supply is V_{CC} * I. Thus the total average supply power is

$$P_S = 2V_{CC}I \quad \textbf{....(8)}$$

Equations (7) and (8) can be combined to yield

$$\eta = \frac{1}{4}\frac{\hat{V}_o^2}{IR_L V_{CC}}$$

$$= \frac{1}{4}\left(\frac{\hat{V}_o}{IR_L}\right)\left(\frac{\hat{V}_o}{V_{CC}}\right)$$

Since $\hat{V}_o \le V_{CC}$ and $\hat{V}_o \le IR_L$, maximum efficiency is obtained when

$$\hat{V}_o = V_{CC} = IR_L$$

Note:
The maximum efficiency attainable is 25%. Because this is a rather low figure, the class A output stage is rarely used in high-power applications (>1 W).

Class B Output Stage:

Class B Output Stage consists of a complementary pair of transistors (an npn and a pnp) connected in such a way that both cannot conduct simultaneously. Hence called as Complementary Symmetric Configuration.

Circuit Operation:
When the input voltage v_I is zero, both transistors are cut off and the output voltage v_O is zero. As v_I goes positive and exceeds about 0.5 V, Q_N conducts and operates as an emitter follower. In this case v_O follows v_I (i.e., $v_O = v_I - v_{BEN}$) and Q_N supplies the load current. Meanwhile, the emitter–base junction of Q_P will be reverse-biased by the V_{BE} of Q_N, which is approximately 0.7 V. Thus Q_P will be cut off.

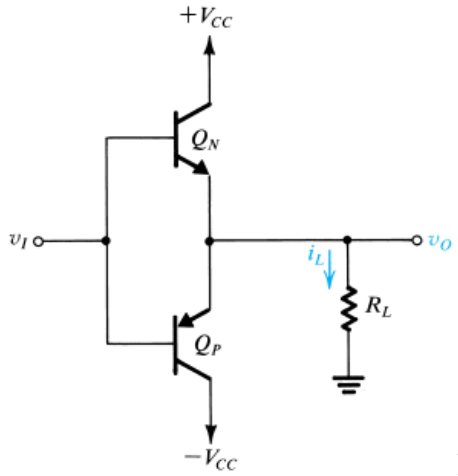


Fig. A class B output stage

If the input goes negative by more than about 0.5 V, Q_P turns on and acts as an emitter follower. Again v_O follows v_I (i.e., $v_O = v_I + v_{EBP}$), but in this case Q_P supplies the load current and Q_N will be cut off.

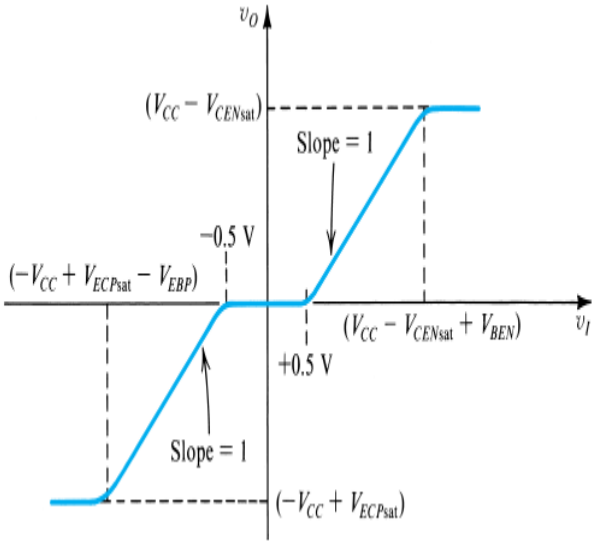
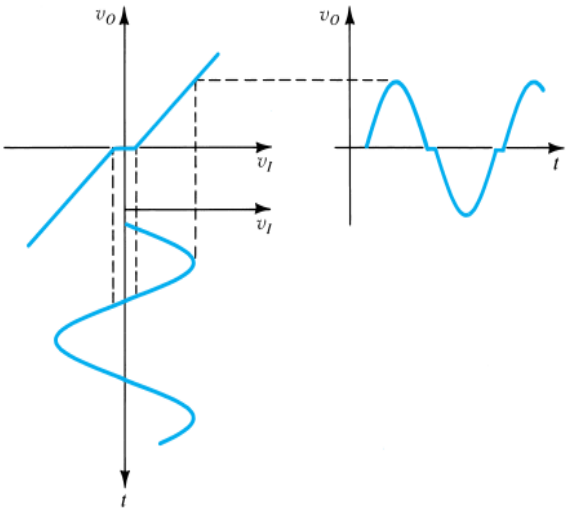


Fig: Illustrating how the dead band in the class B transfer characteristic results in crossover distortion.

Transfer Characteristic:
There exists a range of v_I centered around zero where both transistors are cut off and v_O is zero. This dead band results in the **crossover distortion**.

Fig.: Transfer characteristic for the class B output stage.



Power-Conversion Efficiency:

To calculate the power-conversion efficiency, η, of the class B stage, we neglect the cross-over distortion and consider the case of an output sinusoid of peak amplitude $\hat{V}_o$. The average load power will be,

$$P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L} \quad \text{....(1)}$$

The current drawn from each supply will consist of half-sine waves of peak amplitude $(\hat{V}_o/R_L)$. Thus the average current drawn from each of the two power supplies will be $\hat{V}_o/\pi R_L$. It follows that the average power drawn from each of the two power supplies will be the same,

$$P_{S+} = P_{S-} = \frac{1}{\pi}\frac{\hat{V}_o}{R_L}V_{CC} \quad \text{....(2)}$$

and the total supply power will be

$$P_S = \frac{2\hat{V}_o}{\pi R_L} V_{CC}$$ **….(3)**

Thus the efficiency will be given by

$$\eta = \left(\frac{1}{2}\frac{\hat{V}_o^2}{R_L}\right) \Big/ \left(\frac{2}{\pi}\frac{\hat{V}_o}{R_L} V_{CC}\right) = \frac{\pi}{4}\frac{\hat{V}_o}{V_{CC}}$$ **…..(4)**

It follows that the maximum efficiency is obtained when $\hat{V}_o$ is at its maximum. This maximum is limited by the saturation of Q_N and Q_P to $V_{CC} - V_{CEsat} \simeq V_{CC}$. At this value of peak output voltage, the power-conversion efficiency is

$$\eta_{\max} = \frac{\pi}{4} = 78.5\%$$ **……(5)**

This value is much larger than that obtained in the class A stage (25%). the maximum average power available from a class B output stage is obtained by substituting $\hat{V}_o = V_{CC}$

$$P_{L\max} = \frac{1}{2}\frac{V_{CC}^2}{R_L}$$ **….(6)**

Power Dissipation:

Unlike the class A stage, which dissipates maximum power under quiescent conditions (v_O=0), the quiescent power dissipation of the class B stage is zero. When an input signal is applied, the average power dissipated in the class B stage is given by,

$$P_D = P_S - P_L$$ ….(7)

Substituting for P_S from Eq. (3) and for P_L from Eq. (1) results in

$$P_D = \frac{2}{\pi}\frac{\hat{V}_o}{R_L} V_{CC} - \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$$ ….(8)

Differentiating Eq. (8) with respect to $\hat{V}_o$ and equating the derivative to zero gives the value of that results in maximum average power dissipation as

$$\hat{V}_o\big|_{P_{D\max}} = \frac{2}{\pi} V_{CC}$$ …..(9)

Substituting this value in Eq. (8) gives,

$$P_{D\max} = \frac{2V_{CC}^2}{\pi^2 R_L} \quad \text{....(10)}$$

Thus,

$$P_{DN\max} = P_{DP\max} = \frac{V_{CC}^2}{\pi^2 R_L} \quad \text{....(11)}$$

At the point of maximum power dissipation, the efficiency can be evaluated by substituting for $\hat{V}_o$ from Eq. (9) into Eq. (5); hence, . $\eta = 50\%$.

The figure below shows a sketch of P_D(8) versus the peak output voltage $\hat{V}_o$. It shows that increasing $\hat{V}_o$ beyond decreases the power dissipated in the class B stage while increasing the load power. The price paid is an increase in nonlinear distortion as a result of approaching the saturation region of operation of QN and QP. Transistor saturation flattens the peaks of the output sine waveform. Unfortunately, this type of distortion cannot be significantly reduced by the application of negative feedback, and thus transistor saturation should be avoided in applications requiring low THD.

Reducing Crossover Distortion:

The crossover distortion of a class B output stage can be reduced substantially by employing a high-gain op amp and overall negative feedback, as shown in Fig. below. The ±0.7-V dead band is reduced to volt, where A0is the dc gain of the op amp. Nevertheless, the slew-rate limitation of the op amp will cause the alternate turning on and off of the output transistors to be noticeable, especially at high frequencies. A more practical method for reducing and almost eliminating crossover distortion is found in the class AB stage, which will be studied in the next section.

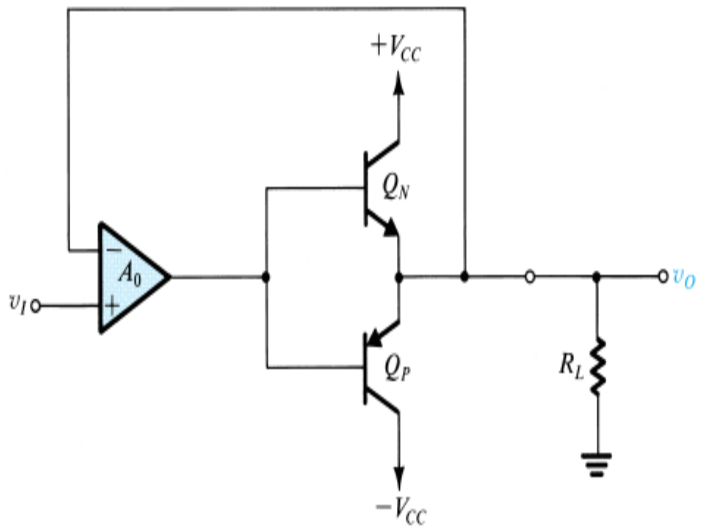


Fig. Class B circuit with an op amp connected in a negative-feedback loop to reduce crossover distortion.

Single-Supply Operation

The class B stage can be operated from a single power supply, in which case the load is capacitive coupled, to make the formulas derived in Dual Supply case directly applicable, the single power supply is denoted $2V_{CC}$

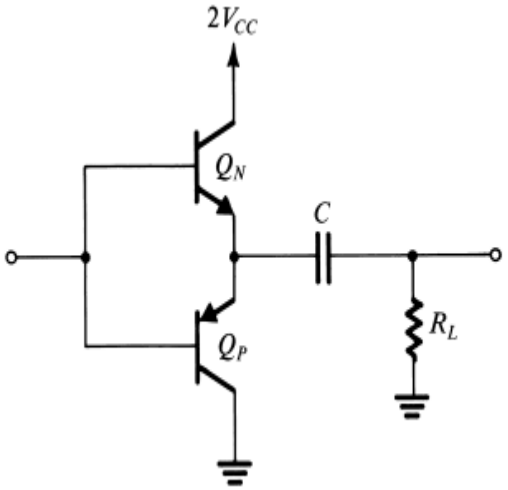


Fig. Class B output stage operated with a single power supply.

Class AB Output Stage:

Crossover distortion can be virtually eliminated by biasing the complementary output transistors at a small nonzero current. The result is the class AB output stage shown in Figure below,
A bias voltage V_{BB} is applied between the bases of QN and QP . For vI =0, vO=0, and a voltage $V_{BB}/2$ appears across the base–emitter junction of each of QN and QP . Assuming matched devices

$$i_N = i_P = I_Q = I_S e^{V_{BB}/2V_T} \quad \ldots.(1)$$

The value of V_{BB} is selected to yield the required quiescent current I_Q

Circuit Operation:
When vI goes positive by a certain amount, the voltage at the base of by thesame amount and the output becomes positive at an almost equal value,

$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEN} \quad \text{....(2)}$$

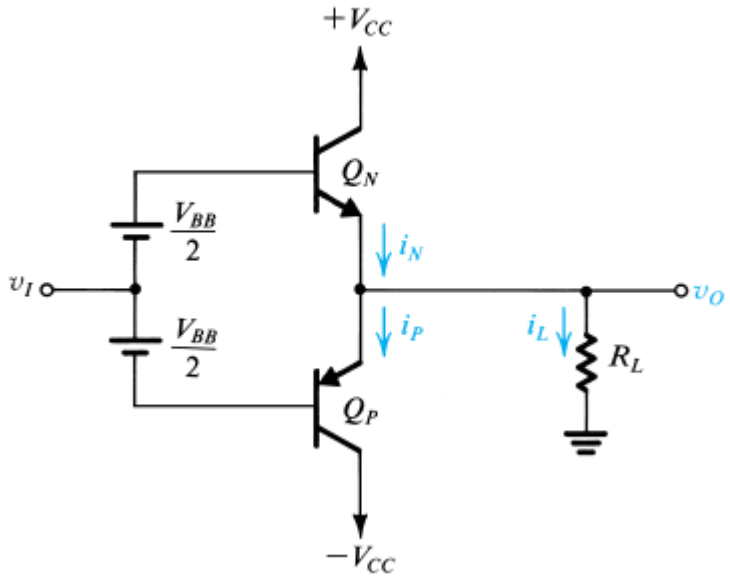


Fig. Class AB output stage

The positive vO causes a current i_L to flow through R_L , and thus i_N must increase; that is,

$$i_N = i_P + i_L \quad \text{..(3)}$$

The increase in i_N will be companied by a corresponding increase in v_{BEN}(above the quiescent value of VBB/2).

$$v_{BEN} + v_{EBP} = V_{BB}$$

$$V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} = 2V_T \ln \frac{I_Q}{I_S}$$

$$i_N i_P = I_Q^2 \quad \text{.....(4)}$$

Thus, as iN increases, iP decreases by the same ratio while the product remains constant.
Equations (3) and (4) can be combined to yield iN for a given iL as the solution to the quadratic equation

$$i_N^2 - i_L i_N - I_Q^2 = 0 \quad \text{....(5)}$$

From the equations above, we can see that for positive output voltages, the load current is supplied by QN, which acts as the output emitter follower. Meanwhile, QP will be conducting a current that decreases as vO increases; for large current in QP can be ignored altogether.
For negative input voltages the opposite occurs: The load current will be supplied by QP,which acts as the output emitter follower, while QN conducts a current that gets smaller as more negative.

the class AB stage operates in much the same manner as the class B circuit, with one important exception: For small vI, both transistors conduct, and as vI is increased or decreased, one of the two transistors takes over the operation. Since the transition is a smooth one, crossover distortion will be almost totally eliminated.

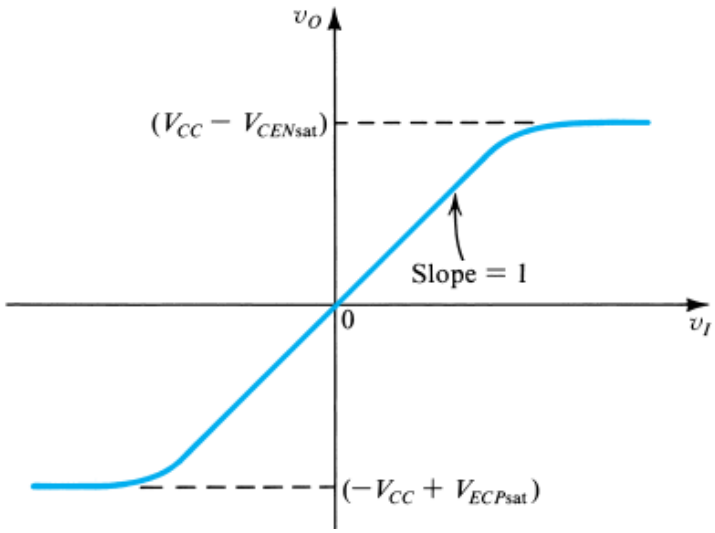
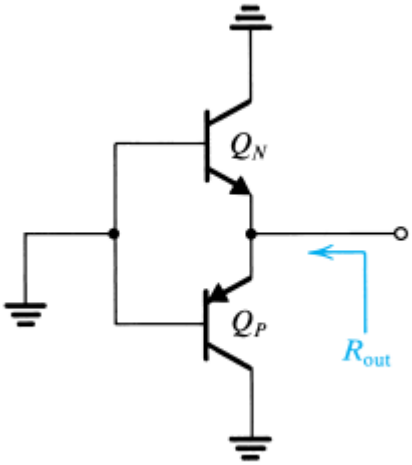


Fig. Transfer characteristic of the class AB stage

Output Resistance:

If we assume that the source supplying vI is ideal, then the output resistance of the class AB stage can be determined

$$R_{\text{out}} = r_{eN} \parallel r_{eP} \quad \ldots.(1)$$



wherere N and Pare the small-signal emitter resistances of QNand QP, respectively. At a given input voltage, the currents iN and iP can be determined, and reNand rePare given by

$$r_{eN} = \frac{V_T}{i_N}$$

$$r_{eP} = \frac{V_T}{i_P}$$

Thus,

$$R_{\text{out}} = \frac{V_T}{i_N} \parallel \frac{V_T}{i_P} = \frac{V_T}{i_P + i_N}$$

Biasing the Class AB Circuit:

There are two approaches for generating the voltage VBB required for biasing the class AB output stage.

1. Biasing Using Diodes
2. Biasing Using the VBE Multiplier

1. Biasing Using Diodes:

A class AB circuit in which the bias voltage VBB is generated by passing a constant current I BIAS through a pair of diodes, or diode-connected transistors, D1 and D2. The biasing diodes, however, need not be large devices, and thus the quiescent current IQ established in QN and QP will be IQ= n* IBIAS, where n is the ratio of the emitter–junction area of the output devices to the junction area of the biasing diodes.

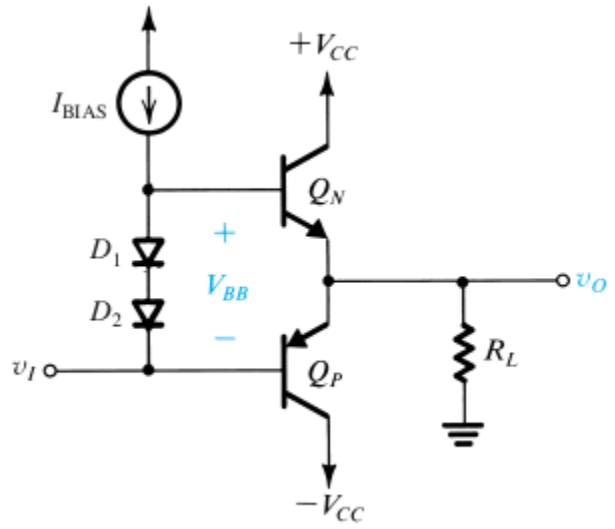


Fig. : A class AB output stage utilizing diodes for biasing

When the output stage of Fig. 11.14 is sourcing current to the load, the base current of QN increases from (which is usually small)to approximately . This base current drive must be supplied by the current source I_{BIAS}. It follows that I_{BIAS} must be greater than the maximum anticipated base drive for QN. This sets a lower limit on the value of I_{BIAS}. Now, since n=IQ / I_{BIAS}, and since IQ is usually much smaller than the peak load current (<10%), it is clear than cannot be a large number. This is a disadvantage of the diode biasing scheme

The diode biasing arrangement has an important advantage: It can provide thermal stabilization of the quiescent current in the output stage. The class AB output stage dissipates power under quiescent conditions. Power dissipation raises the internal temperature of the BJTs. If VBE is held constant and the temperature increases, the collector current increases. The increase in collector current increases the power dissipation, which in turn increases the junction temperature and hence, once more, the collector current. Thus a positive-feedback mechanism exists that can result in a phenomenon called **thermal runaway.**

Diode biasing can be arranged to provide a compensating effect that can protect the output transistors against thermal runaway under quies-cent conditions. Specifically, if the diodes are in close thermal contact with the output transistors, their temperature will increase by the same amount as that of QNand QP. Thus VBB will decrease, with the result that IQ remains constant. Close thermal contact is easily achieved in IC fabrication. It is obtained in discrete circuits by mounting the bias diodes on the metal case of QNor QP.

.

2. Biasing Using the VBEMultiplier:

An alternative biasing arrangement that provides the designer with considerably more flexi-bility in both discrete and integrated designs is shown in Fig. 11.15. The bias circuit consists of transistor Q1with a resistor R1connected between base and emitter and a feedback resistor R2connected between collector and base. The resulting two-terminal network is fed with a constant-current source I_{BIAS}. If we neglect the base current of Q1, then R1and R2will carry the same current I_R, given by

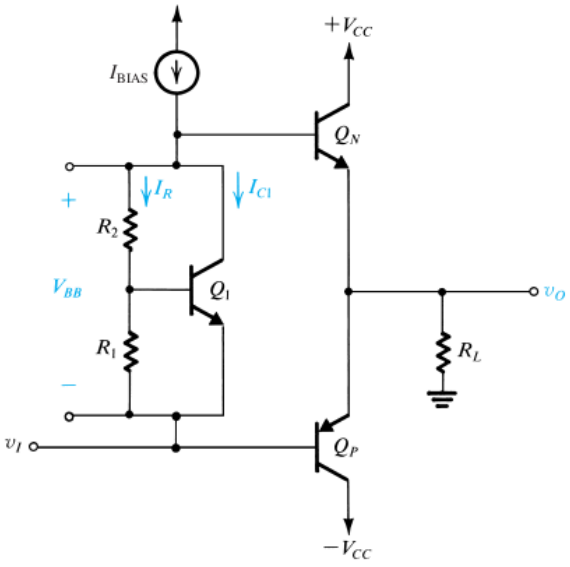


Fig. A class AB output stage utilizing a VBE multiplier for biasing

Thus the circuit simply multiplies VBE1by the factor and is known as the "VBEmultiplier." The multiplication factor is obviously under the designer's control and can be used to establish the value of VBB required to yield a desired quiescent current IQ.

$$I_R = \frac{V_{BE1}}{R_1}$$

and the voltage V_{BB} across the bias network will be

$$V_{BB} = I_R(R_1 + R_2)$$

$$= V_{BE1}\left(1 + \frac{R_2}{R_1}\right)$$

Power BJTs:

Transistors that are required to conduct currents in the ampere range and to withstand power dissipation in the watts and tens-of-watts ranges differ in their physical structure, packaging, and specification from the small-signal transistors.

The important properties of power transistors are,
1. Junction Temperature 2. Thermal Resistance 3. Power Dissipation Versus Temperature (or Power Derating curve)

1. Junction Temperature:
Power transistors dissipate large amounts of power in their collector–base junctions. The dissipated power is converted into heat, which raises the junction temperature. However, the

junction temperature TJmust not be allowed to exceed a specified maximum, TJmax; other-wise the transistor could suffer permanent damage. For silicon devices, TJmaxis in the range of 150°C to 200°C.

2. Thermal Resistance:

Consider first the situation of a transistor operating in free air—that is, with no special arrangements for cooling. The heat dissipated in the transistor junction will be conducted away from the junction to the transistor case, and from the case to the surrounding environ-ment. In a steady state in which the transistor is dissipating PD watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as

$$T_J - T_A = \theta_{JA} P_D \quad \ldots(1)$$

whereθJAis the thermal resistance between junction and ambience, having the units of degrees Celsius per watt. Note that θJA simply gives the rise in junction temperature over the ambient temperature for each watt of dissipated power. Since we wish to be able to dissipatelarge amounts of power without raising the junction temperature above TJmax, it is desirable to have, for the thermal resistance θJA, as small a value as possible. For operation in free air,θJA depends primarily on the type of case in which the transistor is packaged. The value of θJA is usually specified on the transistor data sheet.

Equation (1), which describes the thermal-conduction process, is analogous to Ohm's law, which describes the electrical-conduction process. In this analogy, power dissipation corresponds to current, temperature difference corresponds to voltage difference, and thermal resistance corresponds to electrical resistance. Thus, we may represent the thermal-conduction process by the electric circuit shown in Fig. below.

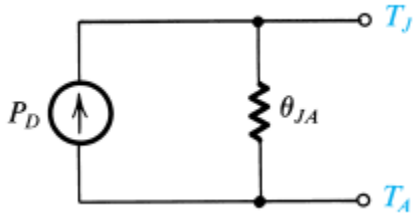


Fig. Electrical equivalent circuit of the thermal-conduction process; TJ− TA= P_DθJA.

3. Power Dissipation Versus Temperature:

The transistor manufacturer usually specifies the maximum junction temperature TJmax , the maximum power dissipation at a particular ambient temperature TA0(usually, 25°C), and the

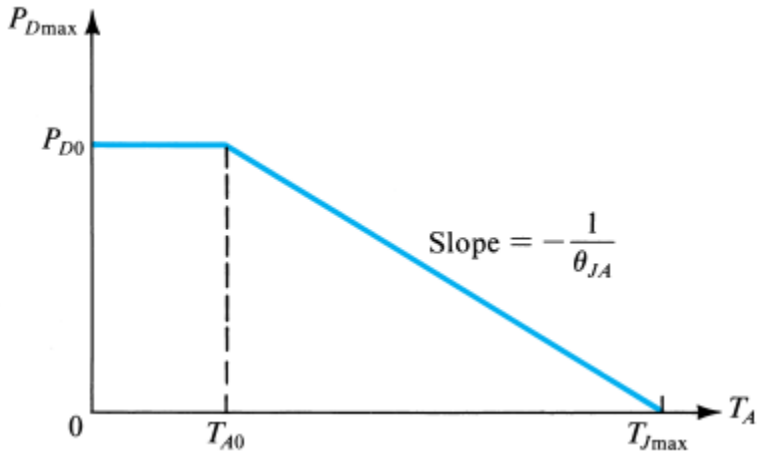


Fig: Maximum allowable power dissipation versus ambient temperature for a BJT operated infree air. This is known as a "power-derating" curve

thermal resistance θJA. In addition, a graph such as that shown in Fig. above is usually provided. The graph simply states that for operation at ambient temperatures below TA0, thedevice can safely dissipate the rated value of PD0watts. However, if the device is to be oper-ated at higher ambient temperatures, the maximum allowable power dissipation must bederatedaccording to the straight line shown in Fig.above. The power-deratingcurveis agraphical representation of Eq. (1). Specifically, note that if the ambient temperature isTA0and the power dissipation is at the maximum allowed (PD0), then the junction temperaturewill be TJmax. Substituting these quantities in Eq. (1) results in

$$\theta_{JA} = \frac{T_{J\max} - T_{A0}}{P_{D0}}$$

which is the inverse of the slope of the power-derating straight line. At an ambient temperatureTA, higher than TA0, the maximum allowable power dissipation PDmaxcan be obtained from Eq. (1) by substituting TJ= TJmax; thus,

Transistor Case and Heat Sink

The thermal resistance between junction and ambience, θJA , can be expressed as

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad \ldots.(1)$$

whereθJCis the thermal resistance between junction and transistor case (package) and θCA isthe thermal resistance between case and ambience. For a given transistor, θJCis fixed by the device design and packaging.

Although the circuit designer has no control over θJC(once a particular transistor hasbeen selected), the designer can considerably reduce θCAbelow its free-air value (specifiedby the manufacturer as part of θJA). Reduction of θCAcan be effected by providing means tofacilitate

heat transfer from case to ambience. A popular approach is to bolt the transistor tothe chassis or to an extended metal surface. Such a metal surface then functions as a heat sink. Heat is easily conducted from the transistor case to the heat sink; that is, the thermal resistance θCSis usually very small. Also, heat is efficiently transferred (by convection and radiation) from the heat sink to the ambience, resulting in a low thermal resistance θSA. Thus,if a heat sink is utilized, the case-to-ambience thermal resistance given by

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

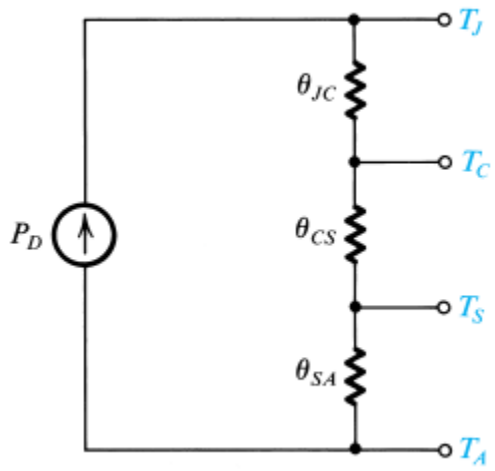


Fig. Electrical analog of the thermal conduction process when a heat sink is utilized.

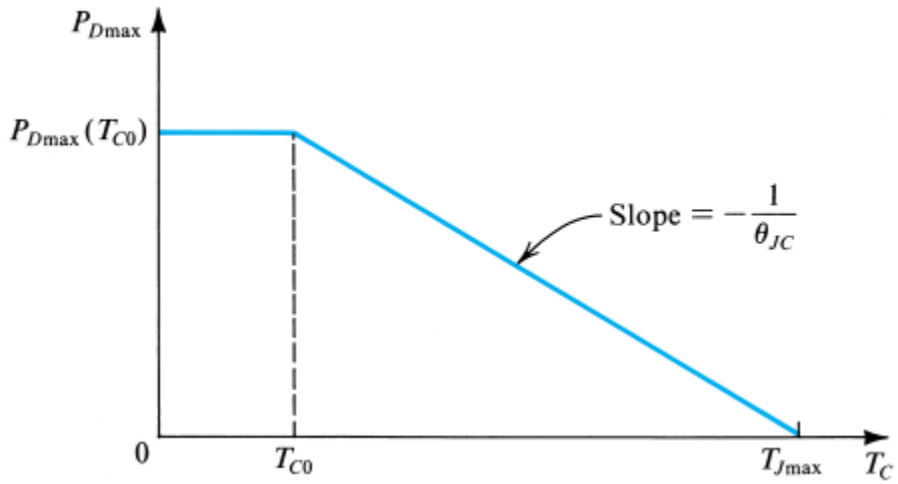


Fig. Maximum allowable power dissipation versus transistor-case temperature

The electrical analog of the thermal-conduction process when a heat sink is employed is

$$T_J - T_A = P_D(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

ASSIGNMENT CUM TUTORIAL QUESTIONS

A. Questions testing his remembering / understanding level of students

I. Objective/ Multiple Choice Questions

1. The Q-point is at cutoff for class _____ power amplifier. [ ]

A) A B) B C) AB D) C

2. What is the maximum efficiency of a class A circuit with a direct

or series-fed load connection [ ]

A) 90% B) 78.5% C) 50% D) 25%

3. Class AB operation is _____ operation. [ ]

A) Similar to Class A B) Similar to Class B

C) Similar to Class C . D) None of the above

4. In _____ power amplifiers, the output signal varies for a full 360º of the cycle [ ]

A) Class A B) Class B C) Class C . D) Class AB

5. In class B power amplifiers, the output signal varies for _____ of the cycle.

6. _____ power amplifier have the highest overall efficiency.

7. Cross over distortion occurs in _____ Power amplifier.

8. Define conversion Efficiency

9. Power amplifiers are large signal amplifiers. [True/False]

10. What is meant by Cross over distortion

11. Which of the following is/are biasing technique for Class AB power Amplifier [ ]

A) Biasing using diodes B) Biasing using V_{BE} Multiplier C) Both A & B D) None

II) Descriptive Questions

1. a) Define Power Conversion Efficiency?
   b) Draw Collector Current waveforms of Class A & Class B , Class AB & Class C Output Stages.
   c) Explain Crossover distortion?
   d) What is Thermal Resistance & Draw its electrical equivalent circuit?
   e) Explain the Thermal resistance property of Power BJTs.

2. a) A BJT is specified to have a maximum power dissipation PD_0 of 5 W at an ambient temperature TA0 of 25°C, and a maximum junction temperature T_{Jmax} of 125°C. Find thermal resistance θ_{JA}.
   b) Draw the Electrical equivalent of Thermal conduction process when Heat Sink is used.
   c) A class B output stage operates with Vcc= 20V , P_L = 15W & average Supply power Ps = 25W. Find η% , Maximum power dissipated at each transistor.
   d) Explain the circuit for reducing cross-over distortion in Class- B Output stage.
3. Explain the Classification of Output Power amplifiers.
4. Detail the operation of Class A Output stage with derivation of Power Conversion efficiency.
5. Derive the expressions for Power Conversion Efficiency & Power Dissipation of Class – B Output Stage.
6. Explain the circuit for reducing cross-over distortion in Class- B Output stage.
7. a) Explain Class- AB output stage biasing using VBE Multiplier circuit.
   b) Explain Class – AB output stage biasing using Diodes.
8. Explain the Significance of Power Derating curve in power BJTs specifications.
9. What is the significance of Heat Sink in power transistors? Explain with the electrical equivalent of Thermal conduction when Heat sink is used.
10. Draw the electrical equivalent of Thermal conduction when Heat sink is used. Explain each term in that.

B. Question testing the ability of students in applying the concepts.

I) Multiple Choice Questions:

1. **An oscillator converts …….** [ ]

A. AC power into DC power

B. DC power into AC power

C. Mechanical power into DC power

D. None of the above

2. In Wein bridge oscillator frequency of oscillation is ……. [ ]

A. Inversely proportional to RC

B. Directly proportional to RC

C. Doesn't depends on RC

D. None of the above

3. **In an LC oscillator, if the value of L is increased four times, the frequency**

of oscillations is …… [ ]

A. Increased 2 times B. Decreased 2 times

C. Increased 4 times D. Decreased 4 times .

4. In **an wein bridge oscillator, if the value of R is increased four times, the frequency of oscillations is ……** [ ]

B. Increases B. Decreases C. Remains the same D. Insufficient data

5. **If the crystal frequency increases with temperature, we say that crystal has …….. Temperature coefficient**. [ ]

A. Positive B. negative C. zero D. none

6. At series or parallel resonance, the circuit behaves as a …….. load

A. Capacitive B. Resistive C. Inductive D. None of the above

II) Problems:

1. For the Class-A emitter follower, V_{CC}=20 V, V_{CEsat} =0.2 V, V_{BE}=0.7 V and constant, and β is very high. Find i) the value of R that will establish a bias current sufficiently large to allow the largest possible output signal swing for R_L=5kΩ. ii) Determine the resulting output signal swing

2. For the Class- A Emitter follower, let V_{CC}=12 V, I =120 mA, and RL=100 Ω. If the output voltage is an 8-V-peak sinusoid, find the following: (a) the power delivered to the load; (b) the Average power drawn from the supplies; (c) the power-conversion efficiency. Ignore the loss inQ3and R.

3. Design a class B output stage to deliver an average power of 15 W to a 8-Ωload. The power supply is to be selected such that V_{CC} is about 5 V greater than the peak output voltage. Determine i) the supply voltage required ii) the peak current drawn from each supply, iii) the total supply power iv) the power-conversion efficiency. v) Determine the maximum power that each transistor must be able to dissipate safely

4. For the class B output stage, let V_{CC}=12 V and R_L=4 Ω. If the output is a sinusoid with8-V peak amplitude, find (a) the output power; (b) the average power drawn from each supply; (c)the power efficiency obtained at this output voltage; (d) the peak currents supplied by v_I, assuming that β_N= β_P=40; (e) the maximum power that each transistor must be capable of dissipating safely

5. A BJT is specified to have a maximum power dissipation PD0of 4 W at an ambient temperature $T_{A0}$of 28°C, and a maximum junction temperature T_{Jmax} of 145°C. Find the following:(a) The thermal resistance θ_{JA}. (b) The maximum power that can be safely dissipated at an ambient temperature of 35°C.(c) The junction temperature if the device is operating at T_A=25°C and is dissipating 4 W.

6. A BJT is specified to have T_{Jmax}=150°C and to be capable of dissipating maximum power as follows: 45W at Tc = 25^{o}C ; 2W at T_A=25^{o}C Above 25°C, the maximum power dissipation is to be derated linearly with θ_{JC}=4.5°C/W and θ_{JA} =65.5°C/W. Find the following:(a) The maximum power that can be dissipated safely by this transistor when operated in free air at T_A=55°C.
7. (b) The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50°C, but with a heat sink for which θ_{CS}=0.4°C/W and θ_{SA}=5°C/W. Find the temperature of the case and of the heat sink.(c) The maximum power that can be dissipated safely if an infinite heat sink is used and T_A=50°C.

C. Question testing his Analyzing/evaluating/Creative abilities of Student

1.) A class B output stage is required to deliver an average power of 100 W into a 16 ohm load. The power supply should be 4 V greater than the corresponding peak sine-wave output voltage. Determine the power –supply voltage required, to the nearest volt in the appropriate direction, the peak current from each supply, the total supply power, and the power conversion efficiency. Also, determine the maximum possible power dissipation in each transistor for a sine-wave input.

2.) The design of a class AB MOS output stage is being considered. The available devices have $|V_n|$ = 1 V and $\mu_n C_{ox} W/L$ = 200 mA/V^2. What value of gate-to-gate bias voltage, V_{GG} is required to reduce the incremental output resistance in the quiescent state to10 Ω.

3.) A particular transistor having a thermal resistance θ_{JA} = 2^{0}C/W is operating at an ambient temperature of 30^{0}C with a collector-emitter voltage of 20 V. If long life requires a maximum junction temperature of 130^{0}C, what is the corresponding device power rating? What is the greatest average collector current that should be considered?.

4.) A power transistor operating at an ambient temperature of 50^{0}C and an average emitter current of 3 A, dissipates 30 W. If the thermal resistance of the transistor is known to be less than 3^{0}C/W, what is the greatest junction temperature you would expect? If the transistor V_{BE} measured using a pulsed emitter current of 3A at a junction temperature of 25^{0}C is 0.80 V, what average V_{BE} would you expect under normal operating conditions? Use a temperature coefficient of -2 mV/^{0}C.

D. Previous GATE/ IES Questions

1. Cross over distortion behavior is a characteristic of **(GATE 2011)**

A) Class A B) Class B C) Class C . D) Class AB

2. A class A transformer coupled transistor power amplifier is required to deliver a power output of 10 watts. The maximum power rating of the transistor should not be less than **(GATE 2012)**

A) 5 watts B) 10 watts C) 15 watts D) 20 watts

3. A power amplifier delivers 50 watts output at 50% efficiency. The ambient temperature is 25^{o}C. If the maximum allowable junction temperature is 150^{o}C, the maximum thermal resistance θ_{JC} that can be tolerated is ---------- **(GATE 2014)**

4. For the 2N338 , the manufacturer specifies P_{max} = 100mW at 25^{o}C , free air temperature and the maximum junction temperature T_{jmax} = 125^{o}C. Its thermal resistance is ----------.**(GATE 2004)**